EDN europe

MARCH 2013
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Issue 3

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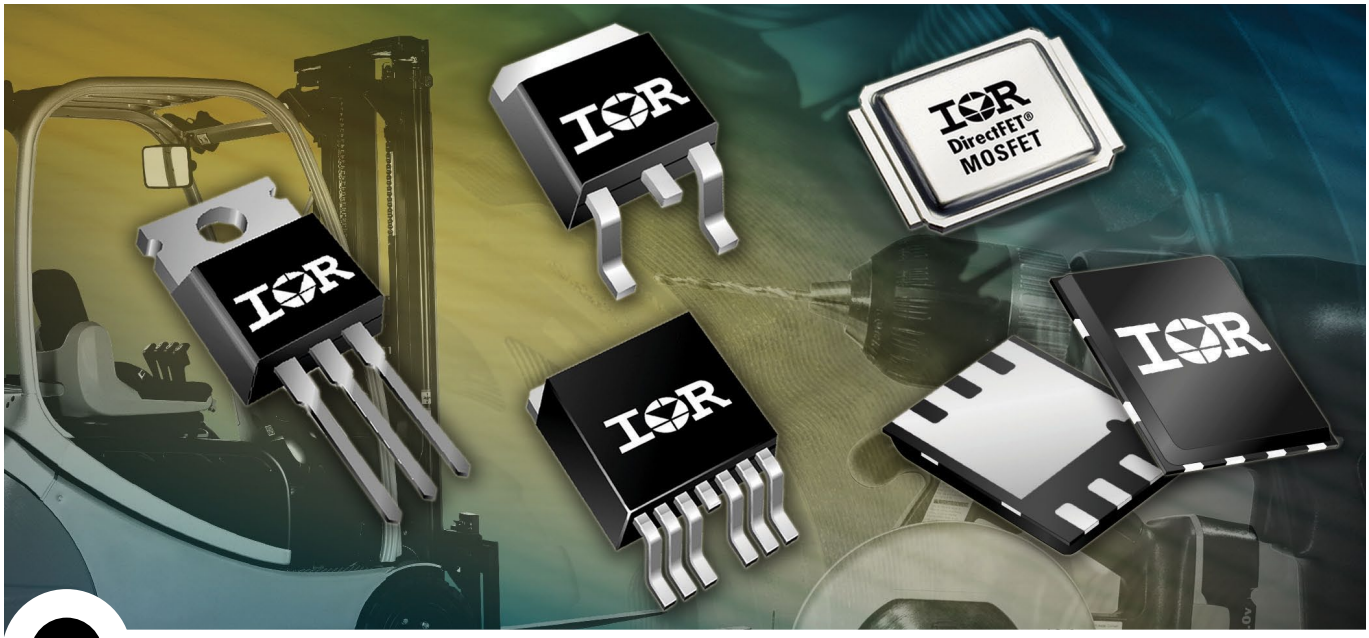

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IRFH7446TRPbF	40 V	85 A	3.3 mΩ	65 nC	PQFN 5x6
IRF7946TRPbF	40 V	90 A	1.4 mΩ	141 nC	DirectFET Medium Can
IRFS7437TRLPbF	40 V	195 A	1.8 mΩ	150 nC	D^2-Pak
IRFS7440TRLPbF	40 V	120 A	2.8 mΩ	90 nC	D^2-Pak
IRFS7437TRL7PP	40 V	195 A	1.5 mΩ	150 nC	D^2-Pak 7pin
IRFR7440TRPbF	40 V	90 A	2.5 mΩ	89 nC	D-Pak
IRFB7430PbF	40 V	195 A	1.3 mΩ	300 nC	TO-220AB
IRFB7434PbF	40 V	195 A	1.6 mΩ	216 nC	TO-220AB
IRFB7437PbF	40 V	195 A	2 mΩ	150 nC	TO-220AB
IRFB7440PbF	40 V	120 A	2.5 mΩ	90 nC	TO-220AB
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Graphics controller cuts cost of embedded displays

Previously known for its range of USB interface chips, FTDI Chip has diversified into the display-controller market with its Embedded Video Engine (EVE), FT800. The company has applied the same principles to the display sector as it did to USB, according to founder Fred Dart; it has packaged up in an easy-to-use form, all of the functions necessary to implement a small display panel, with resistive touch, and has enabled a significant reduction in cost. With the chip at $2.75 (100,000) and a $9 display, you might build in a complete, small, intelligent display for around $15-$17. Dart outlines how, by devising a display controller entirely programmed using object-oriented techniques, expensive elements normally found in a display system, such as a frame buffer, have been eliminated.

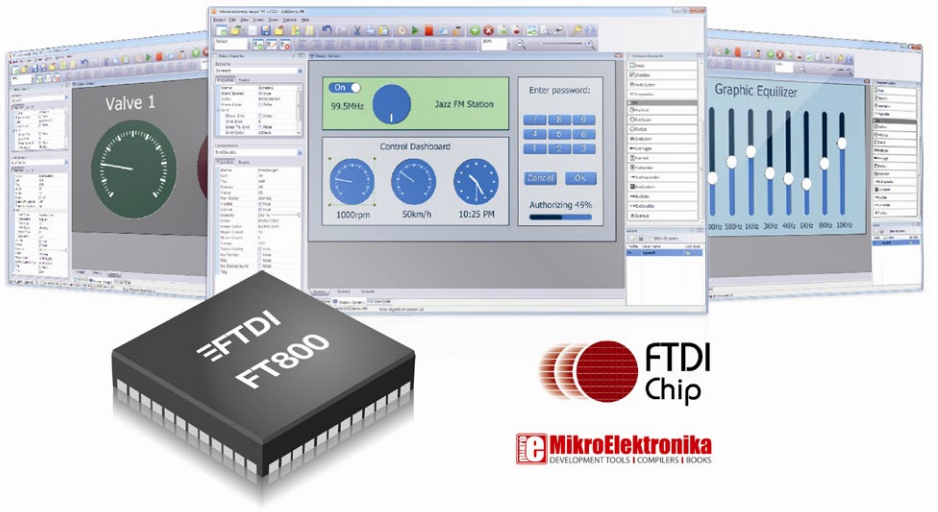
With the FT800, and driving it from a simple microcontroller, you can add an intelligent QVGA or WQVGA TFT display panels to a design. The object oriented approach renders images in a line by line fashion with 1/16th of a pixel resolution. It supports 4-wire resistive touch sensing with built-in intelligent touch detection and an embedded audio processor allowing midi-like sounds combined with pulse code modulation (PCM) for audio playback. The object orientated approach means objects such as images, fonts and audio elements can be easily implemented and manipulated via a low pin-count SPI or I^2C interface. In order for the desired GUI to be realised, you initialise the object memory (up to 256 kBytes) and then control the specified objects and their attributes through construction and interaction of a small display list buffer. As a result of this, even low end (8-bit) MCUs can be used as the host. Up to 2000 objects can be controlled within an 8k byte display list.

The FT800Q is capable of providing 24-bit (true colour) support on an 18-bit interface. It comes preloaded with a useful set of fonts and sounds on its ROM: anti-aliasing mechanisms improve the appearance of the display's output when rendering lines and complex shapes or when implementing signatures on resistive touch screens: in everyday terminology, eliminating "jaggies". Built-in widgets mean that even complex objects (such as analogue clocks) can be implemented with a high quality image. The embedded video engine uses a 36-stage pipeline, with odd/even line buffering.

The chip uses 35 mA (typical) in active mode and 25 µA in sleep mode. It has a -40 to 85°C operational temperature range and is packaged in a 7 x 7 x 0.9 mm 48-lead VQFN package. Dart adds, "With EVE, we are redefining the cost/quality paradigm for GUI development and offering intelligent display solutions with far more competitive price points... for [applications such as] point of sale equipment and printers, while enabling colour touch screen functionality to be added to thermostats, power meters, toys and common home appliances." - by Graham Prophet

FTDT chip, www.ftdichip.com/EVE.htm

Microchip



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MARCH 2013
www.edn-europe.com
Issue 3

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VAT Registration: BE 461.357.437
RPM: Brussels
Company Number: 0461357437

EDN-EUROPE is published 11 times in 2013 by European Business Press SA,
7 Avenue Reine Astrid, 1310 La Hulpe, Belgium
Tel: +32-2-740 00 50 Fax: +32-2-740 00 59
email: info@eetimes.be. VAT Registration: BE 461.357.437.
RPM: Nivelles. Volume 15, Issue 2 EE Times P 304128
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Battery management matters

There's an old joke about the difference between hardware and software engineers that tells of three engineers in a car that suffers brake failure at the top of a hill. They arrive shaken but unhurt at the bottom of the hill; the hardware engineer wants dismantle the braking system and mend it; there's a project engineer in the car and he wants to set a project framework with a scheduled time-to-fix; and there's a software engineer who want to push the car back to the top to see if it does the same again.

It's somewhat tempting to see something of the latter approach in Boeing's troubles with its lithium-ion battery packs, which are still causing all of the new 787s to be parked in corners of various airfields around the world. Meanwhile, Boeing is continuing to produce five new 787s each month, so the parking lot at Seattle must also be getting a bit crowded. At the time of writing this, Boeing (and its contractors) have proposed a solution to allow them to continue to use the same battery chemistry, and have applied to the Federal Aviation Authority to be allowed to flight-test it. The proposal, as far as details have been released, appears to involve placing a little more space and thermal isolation around each cell in the battery pack; enclosing it in a more fire-resistant enclosure; and arranging for that enclosure to be vented to the outside if things go wrong.

What does not seem to have been gained so far is any thorough understanding of why the battery packs in two aircraft suffered "severe overheating events". The history of lithium-chemistry battery development has been long, and a propensity to catch fire has had to be overcome at more than one stage along the way. I recall visiting a factory that was working on Li-ion technology very early, over 20 years ago. At that time the battery structures used much more metallic lithium: that factory was, literally, hard-wired to the local fire department. Later, we had the laptop-battery-fire episodes; and incidents of lithium batteries catching fire while being transported in bulk, while not even in-service.

All of these, the battery technologists have overcome and in one view, Boeing's problems will be just one more step along that path. Reports on the incident on the apron at Boston say that the battery pack was not overcharged beyond its specification. However, it seems unlikely that the pack was at that stage monitored by the aircraft's data recorder down to the level of individual cells, and we know that cell-to-cell equalisation is very important in managing lithium-ion batteries – in fact, in the pages of this issue, you will find news of another novel chip designed to do exactly that. Boeing is opting to persist with taming the Li-ion technology: Airbus (in a not-exactly-equivalent application) has said it will take a step back to NiCd batteries, and accept the lower power density.

Why, some commentators have asked, did Boeing select such a radically new (for a flight-critical system) battery technology? It's a question that does not stand scrutiny; in the course of the design, Boeing had to optimise the weight/performance profile of every aspect of the 787: there would have been no more reason to leave the battery in an older technology than to have held back on, for example, the extensive use of composite materials in the airframe.

In one sense, this is how engineering has always progressed, at its most fundamental level. Analysis is good when you can have it, but sometimes you have to resort to pushing the boundaries and experimenting. Build that arch a little higher, that bridge a little wider – if it falls down, you know your existing technology isn't up to the task, and more research is needed.

We may be sure that when Boeing resumes test flights, those battery packs will be instrumented in every conceivable parameter and, hopefully, will reveal exactly why the existing pack design failed the way it did. The least satisfactory outcome would be that one or more design changes cause the problem to go away, without revealing the fundamental reasons why the failures occurred. There are going to be many more high-density battery packs around us in the near future, and we need to understand them completely.

Meanwhile, it's down to Boeing to push the car back to the top of the hill – or in this case, get back up to 12,000m – and wait to see if it does it again.

[www.edn-europe.com]

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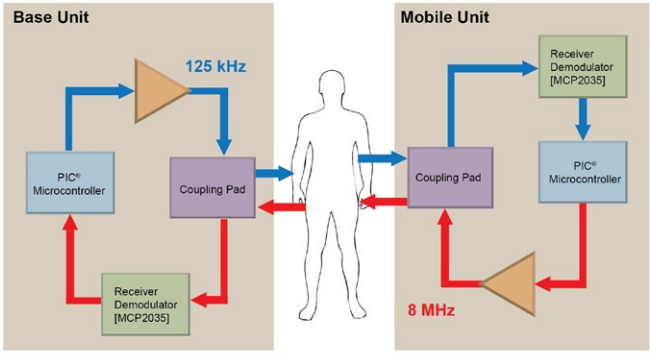
Microchip turns tag into touch

BodyCom technology is a way of using the human body as a secure, low-power communication channel, according to Microchip Technology. Bodycom uses a small, low-power module which you carry on your person. It does not have to be in close contact with the body, carrying it in a pocket is sufficient: but once carried, it enables you to make a "touch" contact with the other part of the BodyCom, a transceiver IC, via an electrode array. By analogy with an NFC tag system, the portable unit turns the user's body into the tag, enabling a low-data-rate exchange (up to 10 kbit/sec) over a very short distance – a touch or proximity contact. You can use it to connect securely to a range of wireless applications, with bidirectional authentication for advanced encryption technologies. Applications can see extended battery life by



eliminating the need for a wireless transceiver or high-power inductive fields. No RF antennas are required, and BodyCom offers simple circuit-level design through use of the BodyCom Development V1.0 Framework, which is supplied through free software libraries that work on all of Microchip's PIC microcontrollers.

BodyCom technology is activated by capacitively coupling to the human body. The system then begins communicating bidirectionally between a centralised controller and one or more wireless units. You can use the scheme, Microchip suggests, as the basis of a highly-secure channel with bidirectional authentication supporting advanced encryption, such as KeeLoq technology and AES. BodyCom technology helps to prevent the "Relay Attack" problem that is typical in automotive passive-keyless-entry security systems, Microchip adds.

The list of possible uses is long, but includes keyless entry; enabling or disabling potentially harmful devices such as power tools (the product will only power-up when held by an authorised user); a similar solution for weapons; medical devices; or consumer electronics such as profile management for gaming consoles and exercise equipment. The "terminal" side of the transaction needs only to be equipped with a conductive array that can be touched by the user, similar to any touch-enabled device. The array can be shared with other touch applications; and transparent ITO (indium-tin-oxide) conductors work well. Therefore, any touch-screen device might have authentication added and would only respond to users who themselves carry a validating tag.

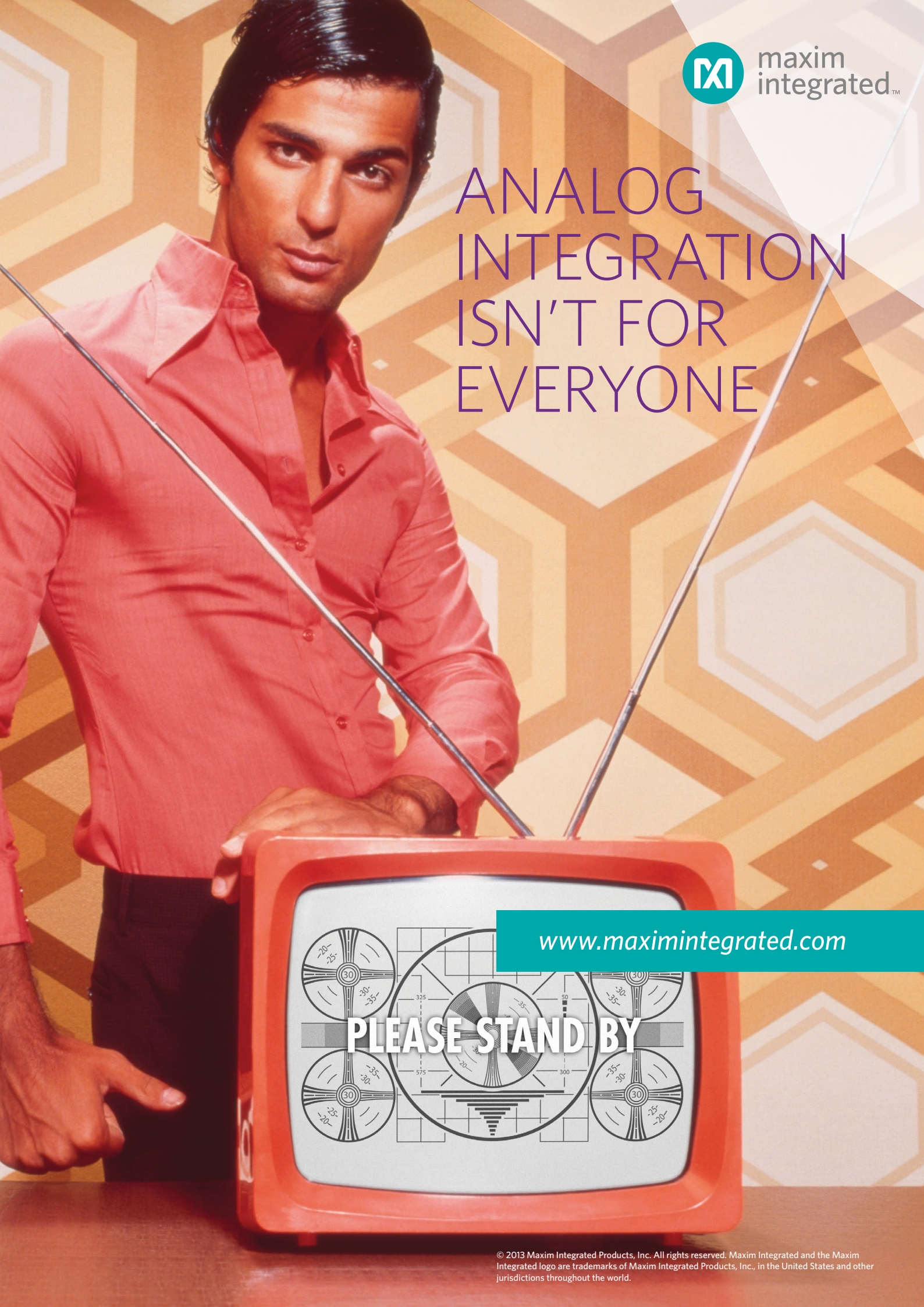
Signals are conducted over the body (from touching finger to pocketed tag) at, Microchip says, picoAmp levels; antenna design is unnecessary, as the systems uses a low-frequency framework with a common microcontroller and standard AFE frequencies (125 kHz and 8 MHz), with no need for external crystals. BodyCom technology also eliminates the cost and complexity of certification because it complies with FCC Part 15-B for radiated emissions.

More at www.microchip.com/get/GA5E

Digitally enhanced power control

Also recently new from Microchip is its digitally enhanced power analogue controller for DC/DC designs – an analogue-based power management controller with integrated MCU, for flexible power conversion; with matching 25-V MOSFETs. Designers of power conversion products who would like to gain the benefits – or at least, some of the benefits – of digital power techniques, without committing themselves to a full-scale digital power design exercise, are offered Microchip's MCP19111. The part marries – on a single die – an analogue power regulator controller, along with a flash-based 8bit PIC microcontroller that carries out configuration, supervisory, reporting and control functions. The part operates from 4.5 to 32V.

Microchip notes that many companies are reluctant to switch to digital power – that is, full digital power designs, where the regulatory control loop is carried out in the digital domain – because of the resource implications of requiring digital design techniques from groups who may not have that expertise. Microchip's solution is to combine its analogue and logic circuitry experience in a single chip; the analogue portion comprises a peak-current regulator controller that drives external MOSFETs via a PWM (pulse-width modulation) generator. Key parameters that, in a fully-analogue part, would be set by external passive components, are controlled by selected values from on-chip switched-arrays of resistors and capacitors. Making that selection is firmware that runs on the associated 8-bit MCU core. The firmware comes with the part, and you set it up via a GUI; no programming is needed. The MCU core has multiple connections into the analogue control loop and can report key voltage and current level, set and monitor thresholds, and report faults over a serial connection. You do not have to write code for the MCU core, but there is capacity to run code if you choose to do so; a Microchip spokesman says that once the power-up configuration is done, the core "has not got much to do" – the computation load that would occupy a DSP or MCU core in a digital part is largely



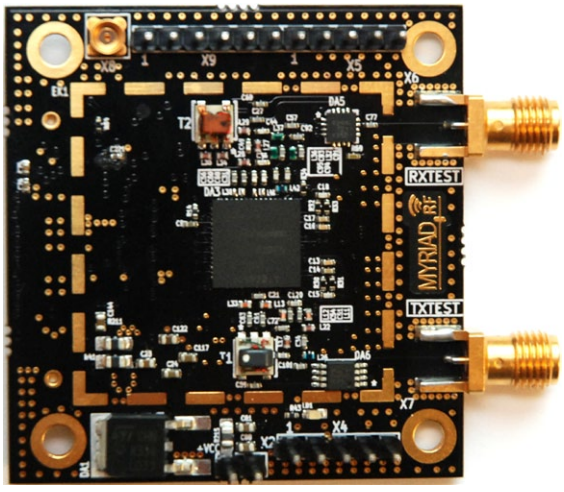
embodied in the analogue loop – and perhaps only 25% of the capacity of the core might be taken up. If you add a PMBus protocol stack to communicate with the digital power bus, that might use 50% of the core's time; but there would still be the capability to implement, for example, a watchdog routine.
There is, however, no facility (or the computational resource) to carry out an auto-compensation routine; as is normal for an analogue regulator, the designer will have to establish the correct loop compensation to achieve stable and responsive behaviour. Once the correct loop filter values have been determined, however, the on-chip microcontroller selects the appropriate R and C values from on-chip arrays: no external parts are needed, and the same base part can be set up with many different values for different applications.
Microchip has been developing its own power output FETs and has released new parts to accompany the 19111 – although the part will drive FETs from other sources. MCP87018, MCP87030, MCP87090 and MCP87130 are high-speed 1.8 mΩ, 3 mΩ, 9 mΩ and 13 mΩ logic-level MOSFETs rated at 25V. Microchip claims a very low (good) figure-of-merit of on-resistance-times-gate-charge; the company notes that, with both controller and MOSFET technology in-house, higher-integration solutions such as multi-FET arrays on a single substrate are a possibility, and Microchip's designers will explore such options as market need dictates. An MCP19111 Evaluation Board (ADM00397) is priced at $49.99 and also includes Microchip's high-speed MOSFETs. It comes with standard firmware, which is user-configurable through an MPLAB X IDE Graphical User Interface (GUI) plug-in. The MCP19111 will cost $2.81 (5000); volume pricing for the FETs ranges from $0.29 to $1.04. - by Graham Prophet
Microchip,
www.microchip.com/MCP19111

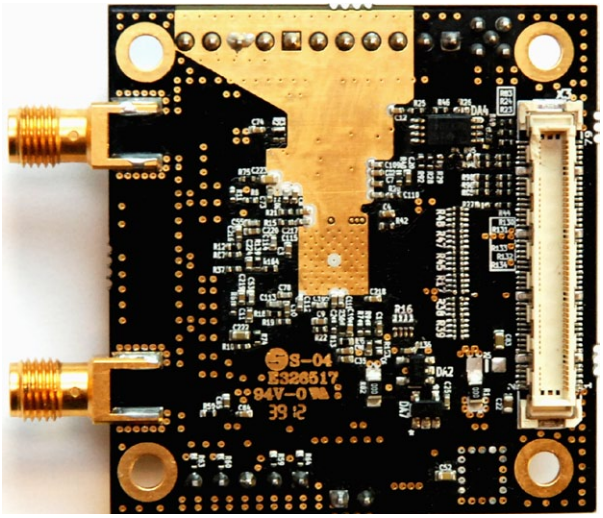
Tanner offers open-access for EDA tool suite

Tanner EDA, popular as a layout and verification tool set among chip designers of medium-scale, mixed signal ASSPs and ASICs, has released version 16 of its HiPer Silicon full-flow design suite, offering designers a complete analogue and mixed-signal design flow from digital (HDL) and analogue (Spice, Verilog-A) electrical design and simulation, through synthesis to physical layout and verification.
Among the changes that Tanner is offering with this release is the OpenAccess database, which the company regards as "[a] most significant development in the semiconductor design tools market".
The objective is to enable customers to use Tanner tools, or any other provider's tool, at any point in the design flow – to step in and out of the the tool chain – with complete tool interoperability while maintaining data in the single database: and to bring a new degree of flexibility and accuracy to process design kits (PDKs) from a variety of silicon foundries. Interoperable PDKs should be usable, Tanner says, with any software flows and with the same common database. Acknowledging that foundries will verify their PDKs against the tool sets of the biggest companies in the sector, Tanner was faced with the task of having its tools interpret all aspects of the design data in the same way. Some of this was specified, the company says, and some had to found by trial-and-error, a lengthy process.
Partly as a consequence of this progress towards an open-access model, version 16 now permits a much higher degree of collaborative and distributed design activity, with team members able to work on the same database with greater ease. Tanner has also added a "traditional" logic design flow to its AMS (analogue/mixed-signal) offering, with HDL through synthesis to layout; synthesis has come from Incentia, and a digital simulator from Aldec has been added. Other enhancements in v16 include; new capabilities for back-end (layout); improved file loading and rendering speeds; improved physical verification (HiPer Verify); new capabilities for front-end (schematic capture, simulation, waveform viewing); integrated mixed-signal simulation (Verilog-AMS co-simulation); plus parametric plots, scatter plots and improved text control and graphics manipulation. - by Graham Prophet
Tanner EDA, www.tannereda.com

Open source RF hardware for wireless innovation

By analogy with the innovation spurred by open-source exemplars such as Linux, and by hardware standards such as Arduino, Lime Microsystems aims to drive innovation in use of the RF spectrum by launching an open-source RF initiative: the non-profit organisation is initially based around a low cost, easy to use, fully configurable RF platform with pre-made boards and free, open, editable design files.
Myriad-RF is a website, aspiring to become an on-line community, that aims to give both experienced design engineers and hobbyists a range of low-cost RF boards and free design files available for general use. Future board designs will come from the wider Myriad-RF community, with the first board (Myriad-RF 1) designed by Taiwanese distributor Azio Electronics.
Lime markets highly integrated, single chip programmable transceivers, that you can set up to work in any one of a wide span of RF bands, with multiple modulation schemes, and with any suitable baseband signalling. In effect, its product is a software-defined-radio-on-a-chip. Its first product (LMS6002D) reached production in late 2010 and the company claims a





customer base of around 150, with several product designs having reached production. These are typically from sectors such as small-cell basestation makers, where experienced RF designers were among the first to exploit the chip's capabilities. However, Ebrahim Busherhi, Lime CEO and instigator of Myriad-RF, believes that the ease-of-use of configurable RF technology should be a platform on which a diverse array of new product concepts can emerge, and that the open community approach may be the way to further that aim. Myriad-RF boards use field programmable RF (FP-RF) transceivers to operate on all mobile broadband standards – LTE, HSPA+, CDMA, 2G – including all regional variants; and any wireless communications frequency between 0.3 and 3.8GHz. This includes the regulated, licensed bands and unlicensed/whitespace spectra. Lime has also beta-launched the Myriad-RF community website and forum, www.myriadrf.org. This resource will also house the board design files and example projects with how-to guides and the ability for users to contribute extra content. All of the design files will be open and downloadable – the CAD environment is KiCad (www.kicad-pcb.org).

Designs hosted on myriadrf.org will initially come from Lime and close partners, but Lime seeks to increase involvement and design contribution from the general RF design community – both hobbyists and professional system designers.

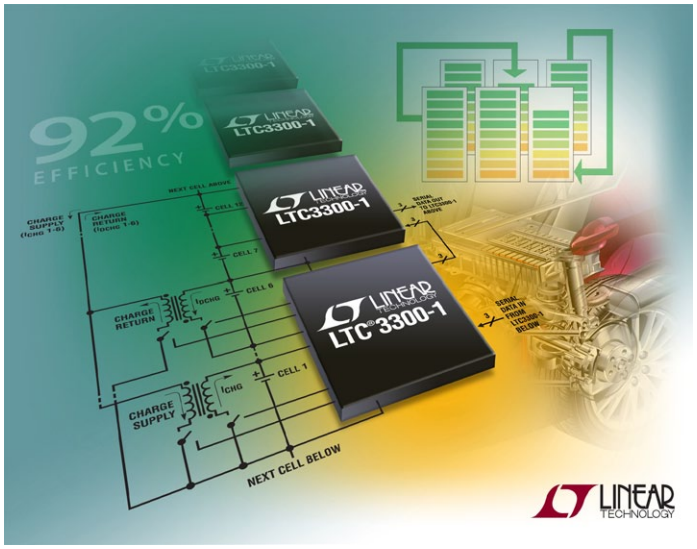
Azio's Myriad-RF 1 board measures approximately 5x5cm, uses a 5V power supply and is software configurable to operate from 300MHz to 3.8GHz and on 2G, 3G and 4G communication networks. Pre-built boards will initially retail for $299 or less: Busherhi hopes this will reduce over time. A distribution network is already in place for pre-built boards and components with Azio Electronics and Eastel already participating. Links to all available pre-built boards can be found on the Myriad-RF board pages. Busherhi mentions ideas such as the possibility of using an FPGA-based baseband board together with a Myriad-RF card, which would provide an environment that would be totally programmable from one end of the signal chain to the other. The Myriad board is, he says, "a simple board with simple connections – you don't have to worry about the RF, it becomes part of the design."

Although Lime Microsystems has an established customer base in areas such as military radio and defence, and in cellular basestations, Busherhi is emphatic that he does not want to restrict activities to any niche sectors; "When we got (our chip) in production, we went broad-market right away, selling it in any quantity to any customer." With Myriad-RF, he hopes to expand that base in the open model. - by Graham Prophet

Lime Microsystems, www.limemicro.com

Multi-cell balancing to increase battery pack performance

Linear Technology's LTC3300-1 is the company's latest IC that addresses the problem of managing the state-of-charge of a multi-cell battery, such as the battery packs in electric vehicles or hybrids (Evs/HEVs). The underlying problem is that cells are never identical and as they age, capacities degrade, and by different amounts in different cells. Unless managed, the capacity of the pack is set by the performance of the lowest-capacity cell. Linear's latest chip balances the cell state of charge in a series-connected battery stack. Many existing solutions carry out balancing by reducing the charge



on higher-charged cells to match the lowest; this optimises the performance of the pack but is inefficient, as the marginal energy is dumped in resistive discharge. LTC3300-1 goes beyond dissipative passive balancing solutions, efficiently transferring charge to or from adjacent cells in order to bring mismatched cells into balance within the stack. Benefits claimed are faster charging and extending the run time and usable lifetime of the battery stack.

You would use the LTC3300-1 in a battery management system (BMS) for series-connected Li-Ion or LiFePO4 batteries. Proposed architectures for active cell balancing include switched circuit arrangements with capacitive or inductive elements, in which some energy is taken from the highest-level cell and passed along the series-connected chain to the lowest. This needs many conversion steps to move a significant amount of charge. Or, there are single-transformer approaches in which the entire pack is switched across, in effect, the primary of a transformer, and the secondary is selectively connected back to the weakest cell. This also requires long balancing times.

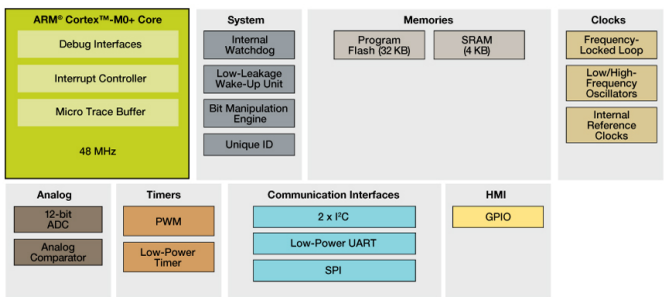
Linear's approach is to use a small transformer per cell with the IC acting as a fault-protected controller IC for transformer-based bidirectional active balancing. The part uses a non-isolated bidirectional synchronous flyback topology to balance up to six series-connected cells. Charge can be transferred to or from a selected cell and 12 or more adjacent cells. All balancers can operate independently and simultaneously with charge/discharge currents up to 10A. Bidirectional operation and simultaneous balancing minimises the time required to equalise the stae-of-charge in the stack, and the parts' high transfer efficiency (up to 92%) enables high current balancing with minimal power dissipation.

You control each individual balancer via a level-shifting SPI-compatible serial interface which enables multiple LTC3300-1 devices to be connected in series, without optocouplers or isolators – this is an approach Linear has developed with previous cell-balancing ICs. Linear has, previously, introduced precision monitor ICs such as the LTC6803-1, that have the dynamic range to accurately measure the small increments that represent state-of-charge differences. The part's stackable architecture together with interleaved transformer connections enable efficient balancing of every cell in an arbitrarily long string of series-connected batteries, even at the level of packs with a voltage of over 1000V. The chip integrates all associated gate drive circuitry, precision current sensing, fault protection circuitry and serial data interface, together with watchdog timer and cyclic redundancy check (CRC) data error checking are integrated. It comes in thermally-enhanced surface-mount compatible packages: a low profile (0.75mm) 48-lead 7 x 7mm QFN and a 48-pin 7 x 7mm LQFP package. Operating junction temperature range is -40°C to +125°C and the part costs $5.95 (1000).

www.linear.com/product/LTC3300-1

Smallest ARM-based MCU, claims Freescale

Kinetis KL02, packaged in an outline of 1.9 x 2.0 mm lays claim to being the smallest-available microcontroller with an ARM core: Freescale intends that you use it in small, connected devices or the "Internet of Things" - or any space- and power-constrained application. The chip hosts an ARM Cortex-M0+ processor, configured with analogue and communication peripherals. Small physical size is enabled by use of wafer-level chip-scale packaging (CSP) that connects the die directly to the solder ball interconnects and, in turn, to the PCB. This, Freescale observes, removes the need for bond wires



or interposer connections, reducing die-to-PCB inductance and improves thermal conduction and package durability for physically harsh environments. The KL02 device is the third CSP MCU in the Kinetis portfolio, joining the larger 120/143-pin Kinetis K series K60/K61 variants. The KL02 sets a new minimum power level for the Kinetis family at 15.9 CM/mA; that is, the benchmark "CoreMark 1.0" rating – the conditions under which this was measured are profiled in the note below. Rated otherwise, Freescale puts the performance at 50 µA/MHz with a 4-µsec wake-up time.

Kinetis KL02 has sufficient processing power for complex algorithms, commuications stacks and human-interfaces, Freescale asserts: the chip also includes autonomous, power-aware peripherals (in this case, an ADC, UART and timer), 10 flexible power modes and extensive clock and power gating to minimise power loss. A low-power boot mode reduces power spikes during the boot sequence or deep sleep wake-up. This is useful, Freescale says, for systems in which battery chemistry limits the allowable peak current, such as those employing lithium-ion batteries frequently used in portable devices. On-chip is a 48-MHz ARM Cortex-M0+ core, operating over 1.71 to 3.6V; a bit manipulation engine for faster, more code-efficient bit-oriented mathematics; 32 KB of flash memory and 4 KB of RAM; a fast 12-bit ADC and a fast analogue comparator; and a range of low-power serial interfaces. There are also timers for applications including motor control.

You can develop systems on the "stackable" Freedom/Tower platform, with access to all of the usual sources of ARM code development tools. There is a software generation tool for creating device drivers and writing start-up code (Processor Expert/Solutions Advisor) and you can use Freescale's MQX real-time operating system.

Rated for operation over -40 to +85C, the chip begins sampling now and will be in production in July 2013: volume (100k) pricing is $0.75.- by Graham Prophet

CoreMark 1.0 configuration: 108.69/IAR for ARM V6.50 --debug --endian=little --cpu=Cortex-M0 -e --fpu=None -Ohs --use_c++_inline/Code in internal FLASH, Data in internal RAM, Stack/Processor operating frequency = 48MHz, operating voltage 3.0V

Freescale, www.freescale.com/Kinetis/KL02CSP

Intel steps up support for industrial control designs

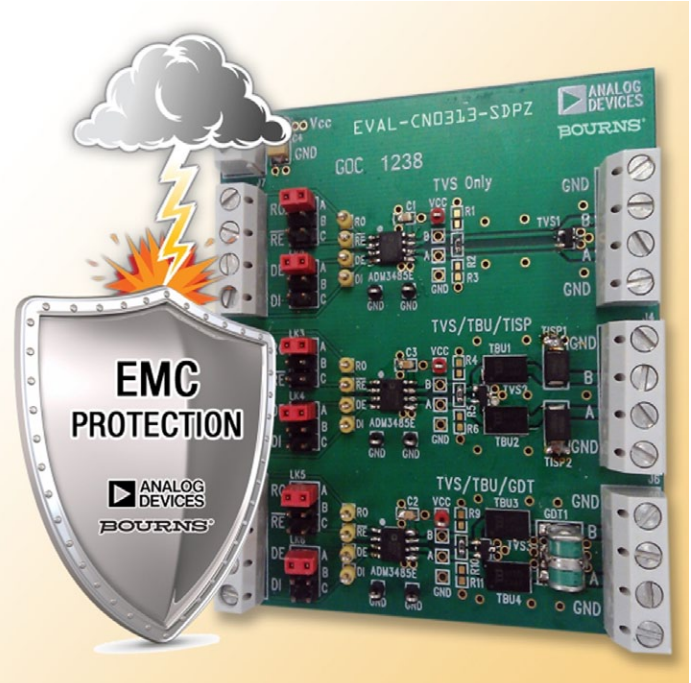
Intel has made a number of introductions around its Intelligent Systems Framework (ISF) including framework-ready products and two new software tools intended to support designers in the industrial market. One specific development is that of a PROFINET IO solution based on the Intel Ethernet Controller I210 and stacks from KW-Software, that achieves the highest level of PROFINET performance. The most common design practice has been to implement the PROFINET interface in an ASSP or an FPGA, Intel says; this development allows the

Intel's System Studio development environment generates a cycle-by-cycle plot of predicted power demand against program flow, to reveal where coding generates highest energy usage.

function to be brought into a standard chipset.
At the same time, Intel is releasing two new software tools – System Studio and the Firmware Support Package – to support ISF. System Studio integrates multiple development tools into a single package aimed at embedded and mobile software developers using Intel processors and SoCs. System Studio includes system and application debuggers, a memory and thread error checker and tools to optimise code for power efficiency (figure) and performance.
The Firmware Support Package provides low-level Intel CPU, Intel chipset and memory firmware initialisation capability using a standardised interface. Previous firmware solutions for embedded devices were, Intel says, highly customised and offered no backward compatibility: you can integrate the Firmware Support Package into any boot loader of the your choice, such as coreboot, Wind River VxWorks, BIOS, Real-Time Operating Systems, Linux and open source firmware.
The Intel System Studio single user licence is available for $3,499 and a floating license
(one seat) is available for $5,299. The Firmware Support Package and the Intel Intelligent
Systems Framework are available free of charge. - by Graham Prophet
Intel, www.intel.com

Design RS485 links with assured EMC protection

Analog Devices has collaborated with Bourns – as a supplier of circuit protection devices – to offer what both companies claim is the first RS485 evaluation board with Certified RS-485 EMC performance. The challenge of matching the EMC characteristics of external protection devices and the components they are designed to protect is, ADI asserts, among the biggest contributors to schedule and cost overruns for manufacturers of industrial and instrumentation equipment. As the externally-certified, EMC-compliant design tool for RS-485 circuits, the EVAL-CN0313-SDPZ board provides design and integration files, device drivers, and evaluation hardware that you can import directly into a target project. The EVAL-CN0313-SDPZ also includes an EI3 Hirose connector that allows the board to be used with ADI's ezLINX iCoupler Isolated Interface Development Environment, giving you a plug-and-play method to evaluate the digitally-isolated RS-485 physical communication layer.
The board incorporates ADI's ADM3485E, 3.3-V RS-485 transceiver and various circuit protection devices from Bourns and meets IEC61000-4-2/4/5 ESD (electro-static discharge), EFT (electronically-fast transients), and power-surge specifications. Specifically, the board offers line protection against 6-kV, 4-kV and 1-kV surges (IEC61000-4-5); 2-kV EFT and 8-kV contact (IEC61000-4-4); and 15-kV air-discharge ESD (IEC61000-4-2). It comes in ADI's "Circuits from the Lab" reference circuits library and includes circuit notes, test data and results that you can apply to applications such as motor controls, mains-connected inverters, and programmable-logic controllers. The development board will cost $78: there will be a webcast on March 27th 2013, details at; www.analog.com/RS485EMC-Webcast
There is a video clip at; www.analog.com/RS485emc
- by Graham Prophet
Analog Devices, www.analog.com/RS485emc



BY BONNIE BAKER

What does "rail to rail" output operation really mean?

The advertisements for single-supply operational amplifiers often claim rail-to-rail output capability. What does this assertion really mean? Page one of a single-supply op amp's data sheet may call out "rail-to-rail input/output swing" in the title or bullets; read on, because if you are looking for a single-supply amplifier whose output can be driven all the way to one supply rail and/or the other, good luck. So, what should you know about an amplifier's performance that claims rail-to-rail output operation?

Two amplifier specifications will help you sort out this problem: output-voltage swing and open-loop voltage gain.

The output-voltage swing of an op amp defines how far you can drive the amplifier output toward the positive or negative supply rail. The output-voltage-swing high (V_{OH}) and output-voltage-swing low (V_{OL}) test conditions usually take the amplifier outside its linear region. The amplifier's open-loop-voltage-gain (A_{VOL}) specification primarily is the ratio of the closed-loop, output-voltage change to the input-offset-voltage change, but it also provides output-linearity hints in the test conditions.

The V_{OH} and V_{OL} specifications tell us how close the output pin comes to the power-supply rails. Figure 1 shows a single-supply amplifier's output behavior. The output stage's transistors prevent the amplifier from reaching either rail.

As you examine these specifications with respect to their test conditions, you will find that the amplifier's output swing is dependent on the amount of current that the output stage is driving into the load. As you can see in Table 1 (Amplifier A), viewable in the online version of this article at www.edn.com/4404550, the defined conditions of this specification have a significant influence on the amplifier's output performance. As the table shows, V_{OH} is the difference between V_{DD} (positive supply). V_{OL} is the difference between the minimum voltage out and V_{SS} (negative supply).

The key to comparing V_{OH} and V_{OL} from amplifier to amplifier is to determine the sink or source current. Smaller output currents provide better output-swing performance.

V_{OH} and V_{OL} tell us how close the amplifier drives to the rails but do not imply that the amplifier is linear so close to the supply voltage rails; the conditions of the A_{VOL} specification, by contrast, do. Measure A_{VOL} by comparing the amplifier's output swing in its linear region with the amplifier's input offset voltage. The dc open-loop gain is equal to the following equation:

$$A_{VOL}=20*\log(\Delta V_{OUT}/\Delta V_{OS}),$$

where ΔV_{OUT} is the dc change in output voltage and ΔV_{OS} is the dc change in input offset voltage.

Table 2 (Amplifier B), also at www.edn.com/4404550, shows an example of the A_{VOL} specifications and test conditions for a single-supply amplifier. In the condition column, note that the high and low output ranges of the amplifier are 5 mV from the power supplies. The A_{VOL} specification verifies that the amplifier is in its linear region.

If you are looking at a single-supply op amp that's claimed to offer rail-to-rail operation, make sure you look deeper before using the product in your application. Consider the V_{OH}, V_{OL}, and A_{VOL} specifications and conditions. Doing so will keep you from wasting your time and will ensure that you have the correct amplifier for your circuit. EDN

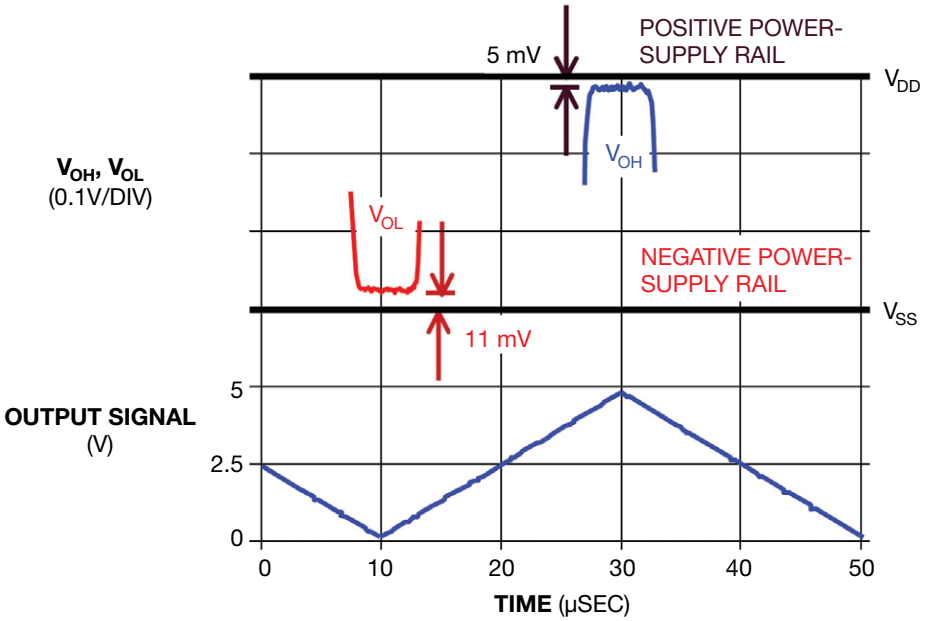


Figure 1 The output signal ramping from V_{SS} (GND) to the positive power supply (V_{DD}=5V) never reaches either rail. At ground, the amplifier stops at ~11 mV from the rail; at V_{DD}, the amplifier stops at ~5 mV from the rail.

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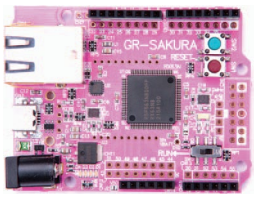

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SIGNAL-INTEGRITY ISSUES ON THE RISE

JANINE LOVE • EDITOR IN CHIEF, TEST & MEASUREMENT WORLD

OUR VIRTUAL PANEL SHARES EYE-OPENING ADVICE FOR ANTICIPATING, DETECTING, AND MITIGATING SI PROBLEMS IN FASTER, INCREASINGLY COMPLEX DESIGNS.

Electronics design trends that ratchet up design complexity and speed, such as the use of multiple high-speed buses, bring new signal-integrity challenges. With that in mind, EDN assembled a virtual panel of engineers working in signal integrity to examine the current impairments, assess how well the available test equipment is measuring up, and determine what we can do both short- and long-term to improve signal integrity. Admittedly, there are many things that can affect signal integrity (Reference 1); in this discussion, we focus primarily on crosstalk and EMI.

WHAT'S THE PROBLEM?

Many a trained eye is focused on the effects of multiple high-speed buses on signal integrity and how to avoid the related problems.
Chris Loberg, senior technical marketing manager at Tektronix Inc, and Tim Caffee, vice president for design validation and test at Asset InterTech Inc, agree that shrinking operating margins on high-speed buses are contributing to the challenges.

"The design trend is faster serial speeds, above 10 Gbits/sec, with no new cost-effective architecture for improving signal-path accommodation of issues like EMI and crosstalk," Loberg observes. "So, signaling accommodations like equalization must be made to minimize EMI and crosstalk effects, enabling the receiver to accurately determine the serial-bus logic transition."

Loberg notes that interval times—the time between a transition to one or zero—are shrinking; as a result, in a traditional eye diagram used to evaluate transitions, EMI and crosstalk are "closing" the eye. Engineers can no longer effectively evaluate signal integrity, as crossing points and timing-integrity evaluations become much more challenging.

Caffee notes that with each successive generation of high-speed bus, operating margins are gradually shrinking as signal frequencies increase, enabling effects such as jitter, intersymbol interference (ISI), and crosstalk to "create havoc" on the signal integrity of high-speed SerDes and memory channels. Each new step to a higher speed and signaling frequency makes the bus more susceptible to distortions and anomalies that can effectively disrupt traffic and stall system throughput.

The eye diagram in Figure 1 illustrates this point, showing the effects of increasing signal frequencies on three generations of a hypothetical high-speed bus and the resultant, decreasing operating margins on the bus. As frequencies increase, even the slightest distortion can disrupt signaling throughput.

Alan Blankman, product manager for signal-integrity products at Teledyne LeCroy, agrees that higher bit rates (>25 Gbits/sec) and "parallelized serial" standards such as PCI Express (PCIe), 40/100GBase-R, and InfiniBand are contributing to signal-integrity issues. "Faster bit rates require faster edges with higher-frequency content, which results in bigger reflections due to impedance mismatches at connectors, vias, packages, etc.; higher levels of loss; and higher levels of crosstalk and EMI, due to increased coupling to neighboring traces," Blankman says.

Shamree Howard, signal-integrity program manager at Agilent Technologies, adds that faster speeds create issues for accurate data capture, requiring precise triggering. She says jitter measurements are the key to characterizing high-speed digital links, noting, "The measurement of jitter—even if the user is provided a one-button interface—is a sophisticated affair, taking into account clock recovery and knowledge of phase-locked loops, jitter decomposition techniques and assumptions for them, crosstalk and its effects, and waveform statistics that require different approaches" (Reference 2). Howard adds that the Agilent U4154A 4-Gbit/sec AXIe logic-analyzer module can make reliable measurements on eye openings as small as 100 psec × 100 mV (Figure 2).

Howard Johnson of Signal Consulting Inc concurs that circuits at very high speeds are notoriously difficult to probe. "Even in cases when a probe exists that can do the job, you often cannot place the probe at the point in a circuit that you wish to observe," says Johnson. He suggests that the answer is to use cosimulation, or the process of simultaneously developing both a physical circuit and a software simulation of it.

The problem, observes Ransom Stephens of Ransom's Notes, is that, despite new oscilloscope techniques from leading manufacturers, there is no automated way to identify crosstalk unambiguously. The latest test products offer ways to estimate the effect of crosstalk on the bit error rate (BER), but they are all process-of-elimination approaches.

"Avoiding crosstalk is simple in principle but sometimes impossible in practice," Stephens acknowledges. Because crosstalk is caused by jolts of radiation when an aggressor signal makes a logic transition, increasing the rise/fall times will reduce crosstalk. Because it's interference, increasing trace separation has a big effect, too.

"I think that careful differential design is your best bet, though," Stephens offers. "If you can get the differential skew really small and get the two traces nearly on top of each other, then the cancellation from differential signaling has a fighting chance."

AT A GLANCE

Each new step to a higher speed and signaling frequency makes the bus more susceptible to distortions and anomalies that can disrupt traffic and stall system throughput. "Parallelized serial" standards are contributing to signal-integrity issues. Circuits at very high speeds are notoriously difficult to probe.

One way forward is to improve the signal path itself with an optical backplane; another way to improve signal integrity is to trick the signal using equalization approaches to minimize crosstalk.

Many designers are managing crosstalk and EMI through better design practices around the signal path.

Most engineers working on signal-integrity issues agree that simulation is becoming mandatory for high-speed system design.

HOW DO WE IMPROVE SI?

According to Tektronix's Loberg, there are several ways forward. First, change and improve the signal path itself. One way to do that is with an optical backplane; this is happening, but not in the mainstream (think Thunderbolt). Another way to improve signal integrity is to trick the signal using equalization approaches to minimize crosstalk; for instance, you could hard-code the chip or compile FPGA code to equalize the signal. In addition, many designers are managing crosstalk and EMI through better design practices around the signal path.

DESPITE NEW OSCILLOSCOPE TECHNIQUES, THERE IS NO AUTOMATED WAY TO IDENTIFY CROSSTALK UNAMBIGUOUSLY.

Asset InterTech's Caffee proposes that engineers validate signal integrity on the bus during each of the major phases of a system's life cycle, from design to field operation, though he recognizes that this is a challenging approach and thus not a popular one. If detected during prototype-board bring-up, signal-integrity problems could trigger changes in the design; if detected during manufacturing, problems could result in alterations to the production process. If problems are detected in the field as a result of troubleshooting poorly perform-

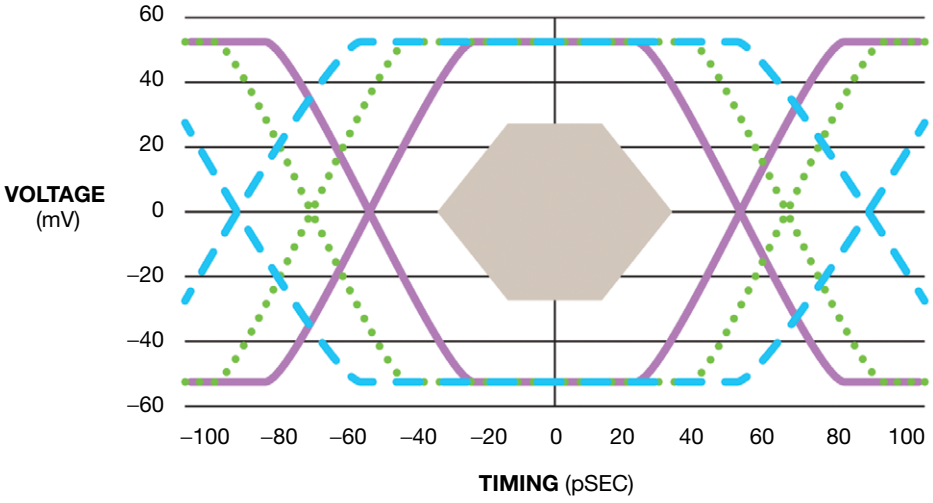

Figure 1 Moving from 6 (broken line) to 8 (dotted line) and, eventually, 10 Gbits/sec (solid line) closes the eye around the operational sweet spot at the center of the diagram (courtesy Asset InterTech).

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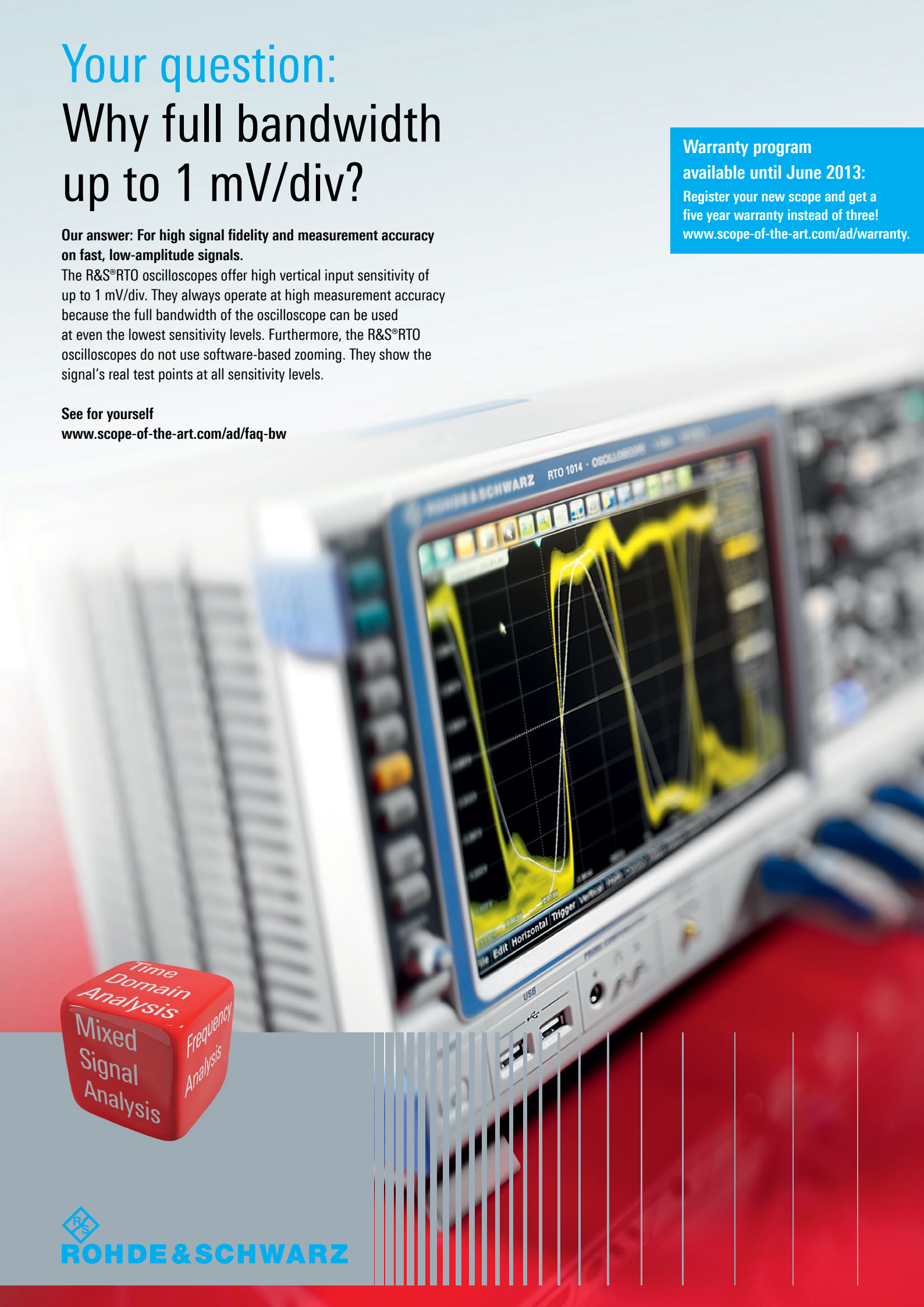

ROHDE&SCHWARZ

ing systems, design changes, manufacturing-process changes, or both should be made for the next product generation to reduce returns and warranty claims.

Hiroshi Goto, business development manager at Anritsu Co, suggests pre-emphasis as an effective transmission technique for maintaining the eye opening. With transmission speeds increasing to 20 Gbits/sec and faster, Goto proposes a three- or four-tap emphasis signal in order to increase the number of bits to be emphasized.

It's a complex job to check and set the combination of emphasis rates for each tap, however, making it difficult to find the ideal emphasis signal without quantitative guidelines.

The Anritsu-developed MP1825B four-tap emphasis and transmission-analysis software, working with the MP1800A signal-quality analyzer BER test set (BERTS), finds "the ideal emphasis settings based upon the reverse characteristics" of the device under test (DUT), says Goto (Figure 3). "This raises the height of the eye and keeps the eye open, allowing better quantitative signal-integrity analysis in the shortest amount of time."

SIMULATION AND VALIDATION

Most agree that simulation is becoming mandatory for high-speed system design. Agilent's Howard says the company's Advanced Design System (ADS) is the leading EDA software in use for high-speed digital applications.

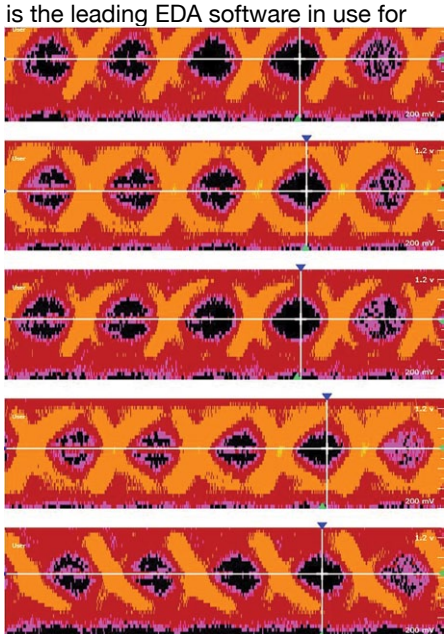

Figure 2 The Agilent U4154A logic analyzer uses its eye-scan capability to place the sampling point automatically in both time and voltage within the eye, making measurements on eye openings as small as 100 psec × 100 mV.

Figure 3 The Anritsu MP1800A 32G synchronized multi-BERTS and MP1825B 28.1G four-tap emphasis aim to assist signal-integrity analysis by keeping the eye open.

Teledyne LeCroy's Blankman adds that to detect and mitigate crosstalk issues, designers must be able to predict near- and far-end crosstalk by running simulations, and to validate the models used in the simulations by taking measurements (Figure 4). To validate crosstalk models, designers need multidifferential-lane S-parameter measurements (eight-port for aggressor-victim models, 12-port for aggressor-victim-aggressor models, or even higher port counts).

Measuring crosstalk requires vertical noise measurements taken by real-time oscilloscopes that can extract the crosstalk from the serial data signal. Those measurements should estimate eye closure as a function of BER, as jitter measurements do. Jitter measurements are also important, of course. Measuring both jitter and noise yields a more complete picture of crosstalk than jitter measurements alone.

TOOLBOX

Test-equipment vendors are working to evolve their tools to characterize jitter and improve signal-integrity analysis, so the optimal toolbox for signal-integrity engineers may not yet be available. Signal Consulting's Johnson predicts that "the next trend will involve a blend of specialized equipment and test software designed to characterize a power system and inject specific test current waveforms into that power system." Stephens, of Ransom's Notes, suggests that we be on the lookout for more crosstalk-equalization techniques.

So, what's out there now?

• Scopes. Here is where high-bandwidth oscilloscopes can really prove their worth. Teledyne LeCroy's Blankman notes that nonreturn-to-zero (NRZ) serial data patterns can have rise times less than 30 psec. He points out that receiver testing of PCIe Gen3 systems requires a

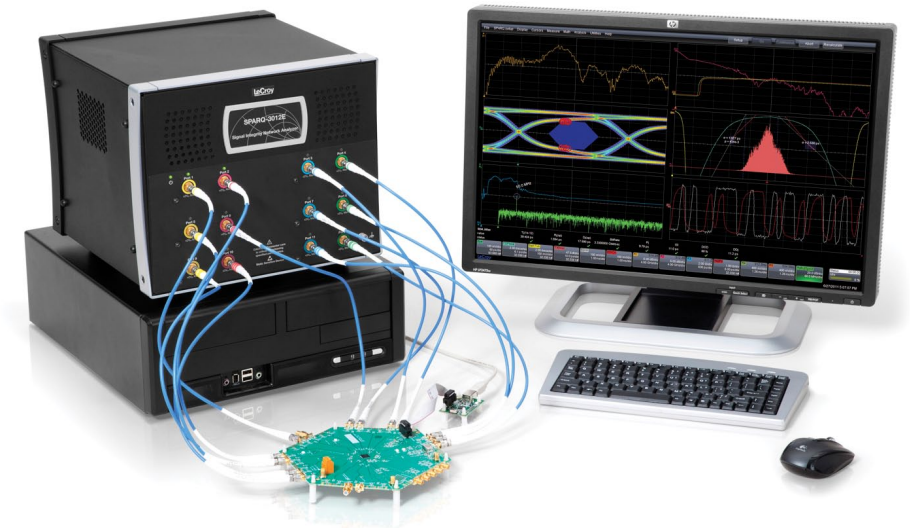

Figure 4 The SPARQ signal-integrity network analyzers from Teledyne LeCroy connect directly to the DUT and PC-based software through a single USB connection for quick, multiport S-parameter measurements.

scope with a 13-GHz bandwidth, whereas transmitter testing needs a 20-GHz scope.

"Emerging multilane designs like InfiniBand and 40/100GBase-R have even more-demanding requirements for channel count and bandwidth," Blankman says. "These standards utilize bit rates of 25 and 28 Gbits/sec. Typically, an oscilloscope with four or five times the fundamental frequency is needed, which corresponds to 50 to 65 GHz. Since InfiniBand and 40/100GBase-R are multilane, acquiring eight, 12, or even more channels at a time is required to fully characterize SI issues." Blankman points to Teledyne LeCroy's LabMaster 10 Zi, with bandwidth out to 65 GHz and a ChannelSync architecture that synchronizes up to 80 channels to operate as a single instrument.

• Network analyzers. Network analyzers are important for characterizing crosstalk in multilane systems and revealing the frequency characteristics of the DUT. Anritsu's Goto points out that in order to acquire the best S-parameter data, the vector network analyzer should have broad frequency coverage. He suggests Anritsu's VectorStar VNA, which ranges from 70 kHz to 125 GHz.

"While the upper frequency receives most of the attention," he warns, "it is important to remember that accurate measurements to the lowest possible frequency are critical for signal-integrity applications. Often, the accuracy of models can be improved by measuring down to as close to dc as possible, providing the precise data to help create a high-accuracy eye diagram."

Blankman notes that network analyzers with high port counts can be expensive. He says the network analyzers in Teledyne LeCroy's SPARQ series (Figure 4) were designed for signal-integrity measurements and offer a lower-cost option to a traditional VNA. (SPARQ stands for "S-parameters quick.")

• Software. Given the need for more simulation, vendors are developing software tools to work with their hardware. Loberg notes the availability of serial-data-link analysis (SDLA) on the Tektronix scope (Figure 5), which can help engineers simulate equalization in EDA environments such as those from Cadence Design Systems or Mentor Graphics. "That software model can be dropped into an oscilloscope, transferring the model properties into the S-parameters; then we can place the effects of that effort into a filter on the scope," Loberg explains. "The scope can then model the behavior of the equalizer into the signal being measured and see if we can open the eye. This approach allows you to analyze the performance with the effects of equalization baked into the scope."

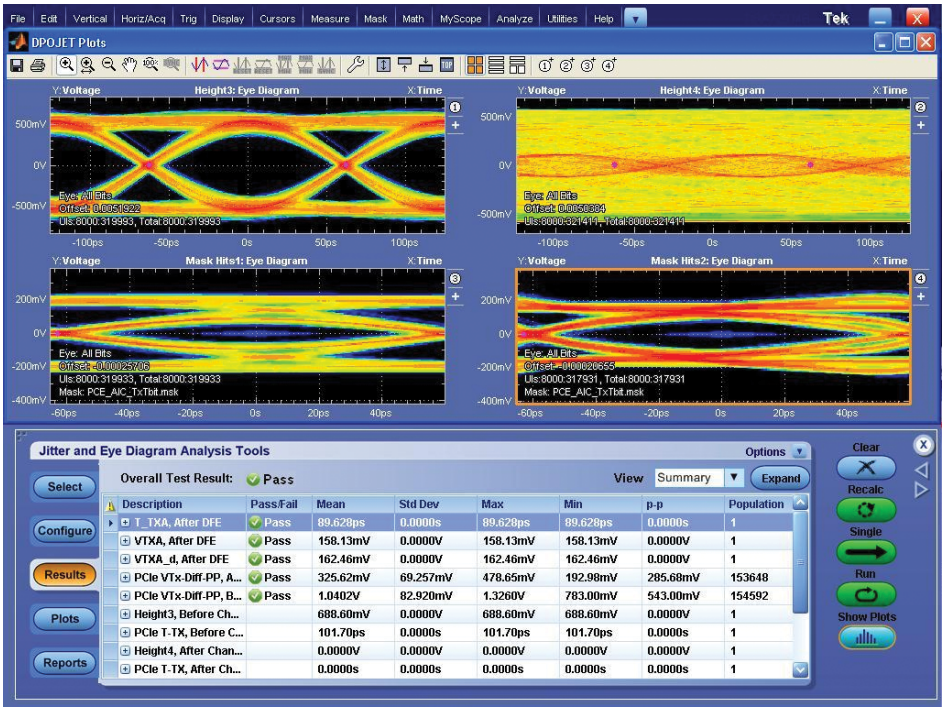

Figure 5 This screen image of serial-data-link analysis shows different eye diagrams before and after inclusion of equalization effects and channel/fixturing effects (courtesy Tektronix).

JTAG PROVIDES ACCESS TO AN EXTERNAL SOFTWARE-BASED PLATFORM THAT CAN MANAGE THE SYSTEM'S EMBEDDED INSTRUMENTS.

Teledyne LeCroy also offers oscilloscope-based serial-data-analysis software in its SDAIII-CompleteLinQ product. Blankman notes that it is important to have scope-based software that performs eye, jitter, and vertical noise analysis. He says users also need tool kits that allow fixtures and interconnects to be de-embedded or emulated, and that apply transmitter and receiver equalization. "The analysis tool kit should also provide a wide variety of plots that show the variation and distribution of jitter and noise in frequency and time in order to understand the root causes of noise and jitter," Blankman adds.

• BERT. "Receiver testing is becoming mandatory in many standards, and most people don't know where to start," says Howard, who adds that system calibration—critical for ensuring the accuracy of your measurements—may be the hardest part of testing.

Howard reveals that in working with engineers, she has found proper calibration of the stress signal in PCIe 3.0 to be challenging. She points to the Agilent N4903B J-BERT high-performance serial BERT to test Rx compliance. The instrument can characterize a receiver's jitter tolerance and is designed to prove compliance with today's most popular serial-bus standards, including PCIe, SATA/SAS, DisplayPort, and USB.

Goto suggests that when selecting a BERT, engineers should choose one with minimal intrinsic jitter. For example, the Anritsu MP1800A has intrinsic clock jitter of <350 fsec RMS. The BERT should also be able to conduct repeatable and stable jitter-tolerance tests with a variety of generated jitter types, such as sinusoidal, random, and bounded uncorrelated jitter and spread-spectrum clock that can be measured up to 32.1 Gbits/sec.

• Embedded test. The days of probing test pads are coming to a close, especially for high-speed buses, because the practice can introduce anomalies into the signal. So where does

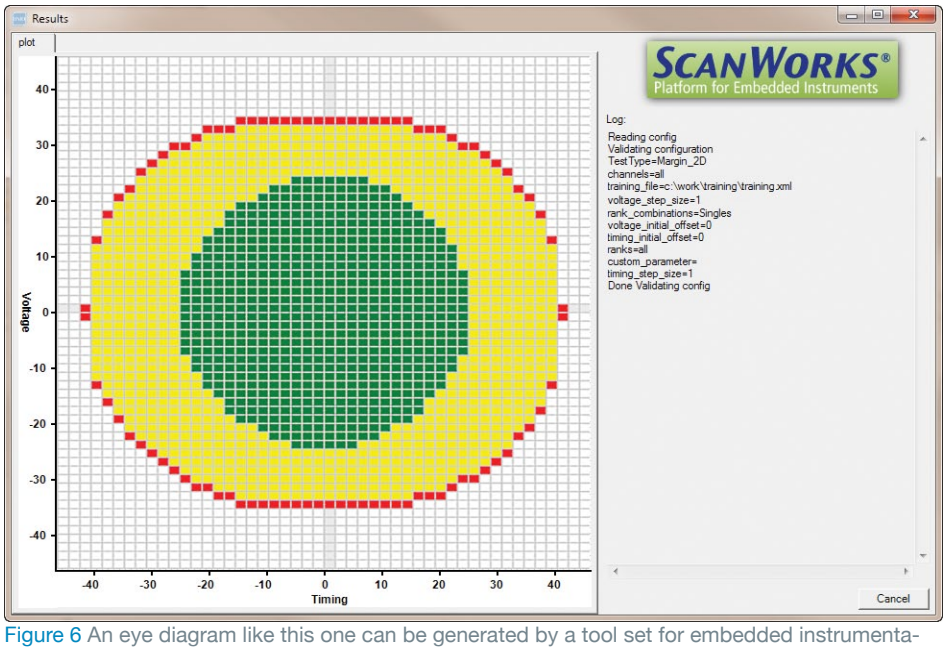

Figure 6 An eye diagram like this one can be generated by a tool set for embedded instrumentation (courtesy Asset InterTech).

that leave us? There is a growing interest in embedded test instruments, and the design-for-test movement is allowing nonintrusive embedded instruments to deliver the signal data that the receivers see. "In other words," says Caffee, "soft access is provided to the hard data that signal-integrity engineers need."

Embedded instruments have been used for years for chip-level characterization, verification, and test. But now, embedded instruments are being used to monitor and report data being received by the receiver. Caffee notes that the embedded instruments are accessed using standard technologies, such as the IEEE 1149.1 boundary-scan (JTAG) test-access port.

"JTAG provides access to an external software-based platform that can manage the embedded instruments in the system, as well as compile and analyze the test and measurement data they gather," Caffee says (Figure 6).

As system speed and complexity continue to rise, the way forward looks to be a combination of advanced measurement tools and techniques that work with customized simulation models. In the end, though, the path of least resistance for improving signal integrity looks to be an industry standby: good old-fashioned engineering ingenuity.EDN

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BY MARK FORTUNATO • MAXIM INTEGRATED

Why your 4.7-µF ceramic cap becomes a 0.33-µF cap

AN INVESTIGATION INTO TEMPERATURE AND VOLTAGE VARIATIONS IN X7R CAPACITORS UNDERSCORES THE IMPORTANCE OF DATA SHEETS.

A few years ago, after more than 25 years of working with ceramic capacitors, I learned something new about them. I was working on an LED-light-bulb driver, and the time constant of an RC circuit in my project simply did not seem to be right.

I immediately assumed that there was an incorrect component value installed on the board, so I measured the two resistors serving as a voltage divider. They were just fine. I desoldered the capacitor from the board and measured that component; the cap, too, was fine. Just to be sure, I measured and installed new resistors and a new capacitor, fired up the circuit, checked that the basic operation was proper, and then went to see whether the component swap had resolved my RC time-constant problem. It had not.

A TEMPERATURE PROBLEM?

I was testing the circuit in its natural environment: in its housing, which itself was in an enclosure to mimic a "can" for ceiling lighting. The component temperatures in some instances reached well over +100°C. Even in the short time it had taken me to retest the RC behavior, things had become quite hot.

My next conclusion, of course, was that the temperature variation of the capacitor was the issue. I was skeptical of that conclusion even as I drew it, however, because I was using X7R capacitors, which to my recollection varied only ±15% up to +125°C. I trusted my memory, but to be sure, I reviewed the data sheet for the capacitor that I was using.

That is when my ceramic-capacitor reeducation began.

BACKGROUNDER

Table 1 shows the letters and numbers used for various ceramic-capacitor types and what each means. The table describes Class II and Class III ceramics. Without getting too deep into details, Class I capacitors include the common COG (NPO) type; these are not as volumetrically efficient as the ones listed in the table, but they are far more stable over varying environmental conditions, and they do not exhibit piezo effects. The capacitors listed in the table, by contrast, can have widely varying characteristics; they will expand and contract with applied voltage, sometimes causing audible (buzzing or ringing) piezo effects.

Of the many capacitor types shown, the most common, in my experience, are X5R, X7R, and Y5V. I never use the Y5Vs, because they exhibit extremely large capacitance variation over the range of environmental conditions.

When capacitor companies develop products, they choose materials with characteristics that will enable the capacitors to operate within the specified variation (third character; Table 1) over the specified temperature range (first and second characters). The X7R capacitors that I was using should not have varied more than ±15% over a temperature range of –55°C to +125°C, so either I had a bad batch of capacitors or something else was happening in my circuit.

TABLE 1 COMMON CERAMIC-CAPACITOR TYPES

First character: low temp		Second character: high temp		Third character: Change over temp (max)	
Char	Temp (°C)	Num	Temp (°C)	Char	Change (%)
Z	10	2	45	A	±1
Y	30	4	65	B	±1.5
X	55	5	85	C	±2.2
–	–	6	105	D	±3.3
–	–	7	125	E	±4.7
–	–	8	150	F	±7.5
–	–	9	200	P	±10
–	–	–	–	R	±15
–	–	–	–	S	±22
–	–	–	–	T	22, –33
–	–	–	–	U	22, –56
–	–	–	–	V	22, –82

NOT ALL X7Rs ARE CREATED EQUAL

Since my RC time-constant problem was far greater than would be explained by the specified temperature variation, I had to dig deeper. Looking at the data for capacitance variation versus applied voltage for my capacitor, I was surprised to see how much the capacitance changed with the conditions I had set. I had chosen a 16V capacitor to operate with a 12V bias. The data sheet indicated that my 4.7-µF capacitor would typically provide 1.5 µF of capacitance under those conditions. Now, that explained the problem my RC circuit was having.

The data sheet then showed that if I just increased the size of my capacitor from the 0805 to the 1206 package size, the typical capacitance under the specified conditions would be 3.4 µF. This called for more investigation.

I discovered that Murata Manufacturing Co (www.murata.com) and TDK Corp (www.tdk.com) offer nifty tools on their Web sites that let you plot the variations of capacitors over different environmental conditions. I investigated 4.7-µF capacitors of various sizes and voltage ratings. Figure 1 graphs the data that I extracted from the Murata tool for several different 4.7-µF ceramic capacitors. I looked at both X5R and X7R types, in package sizes from 0603 to 1812 and with voltage ratings from 6.3 to 25V dc. Note, first, that as the package size increases, the capacitance variation with applied dc voltage decreases—and does so substantially.

A second interesting point is that, for a given package size and ceramic type, the capacitor voltage rating seems often to have no effect. I would have expected that using a 25V-rated capacitor at 12V would result in less variation than using a 16V-rated capacitor under the same bias. Looking at the traces for X5Rs in the 1206 package, it's clear that the 6.3V-rated part does indeed perform better than its siblings with higher voltage ratings.

TABLE 2 CAPACITANCE OF X7R CAPS WITH A 12V BIAS

Size	C (µF)	% of Nominal
0805	1.53	32.6
1206	3.43	73
1210	4.16	88.5
1812	4.18	88.9
Nominal	4.7	100

If we were to examine a broader range of capacitors, we would find this behavior to be common. The sample set of capacitors that I considered in my investigation did not exhibit the behavior to the same extent as the general population of ceramic capacitors would.

A third observation is that, for the same package, X7Rs have better temperature sensitivity than do X5Rs. I do not know whether this holds true universally, but it did seem so in my investigation.

Using the data from this graph, Table 2 shows how much the X7R capacitances decreased with a 12V bias. Note that there is a steady improvement with progressively larger capacitor sizes until the 1210 size; going beyond that size yields no real improvement.

CHOOSING THE RIGHT CAPACITOR

In my case, I had chosen the smallest available package for a 4.7-µF X7R because size was a concern for my project. In my ignorance, I had assumed that any X7R was as effective as any other X7R; clearly, this is not the case. To get the proper performance for my application, I had to use a larger package.

I really did not want to go to a 1210 package. Fortunately, I

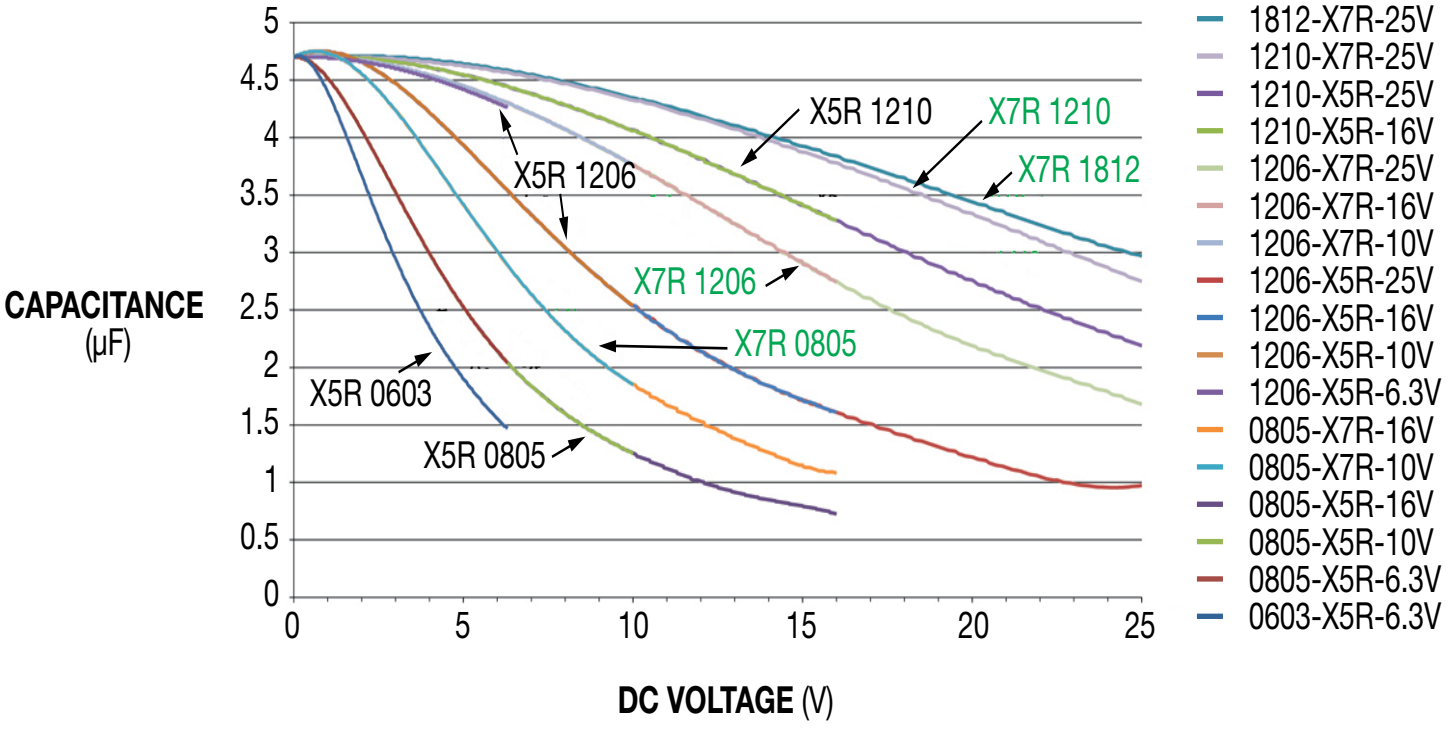


Figure 1 As this graphic representation of temperature variation versus dc voltage for select 4.7-µF capacitors shows, as the package size increases, the capacitance variation with applied voltage substantially decreases.

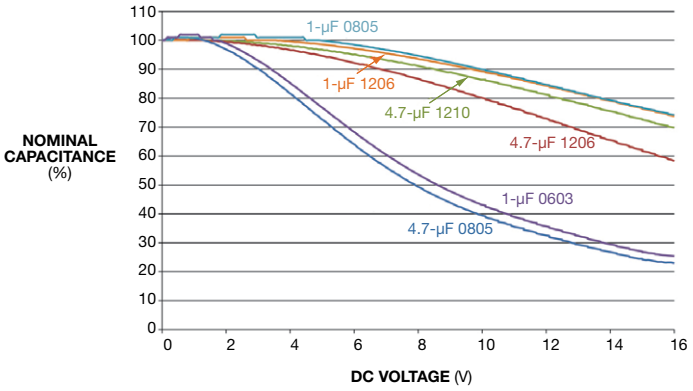


Figure 2 This graph, which plots the voltage performance of 1-µF and 4.7-µF capacitors, shows similar performance for the 1-µF 0603 and the 4.7-µF 0805.

had the freedom to increase the values of the resistors involved by about 5× and thereby decrease the capacitance to 1 µF.

Figure 2 graphs the voltage behavior of several 16V, 1-µF X7R caps versus that of 16V, 4.7-µF X7Rs. The 0603 1-µF capacitor behaves about the same as the 0805 4.7-µF device. Both the 0805 and 1206 1-µF capacitors perform slightly better than the 1210 4.7-µF size. Thus, by using the 0805 1-µF device, I was able to keep the capacitor size unchanged while getting a capacitor that only dropped to about 85% of nominal, rather than 30%, under bias.

But I was still confused. I had been under the impression that all X7R caps should have similar voltage coefficients because the dielectric used was the same, namely X7R. So I contacted a colleague and expert on ceramic capacitors, TDK field applications engineer Chris Burkett, who explained that there are many materials that qualify as "X7R." In fact, any material that allows a device to meet or exceed the X7R temperature characteristics, ±15% over –55°C to +125°C, can be called X7R. Burkett also explained that there are no voltage-coefficient specifications for X7R or any other ceramic-capacitor type.

This is a critical point, so I will repeat it. A vendor can call a capacitor X7R (or X5R, or any other type) as long as the cap meets the temperature-coefficient specs, regardless of how bad the voltage coefficient is. This fact reinforces the old maxim (pun intended) that any experienced applications engineer knows: Read the data sheet!

As capacitor vendors have turned out progressively smaller components, they have had to compromise on the materials used. To get the needed volumetric efficiencies in the smaller sizes, they have had to accept poorer voltage coefficients. Of course, the more reputable manufacturers do their best to minimize the adverse effects of this trade-off.

Consequently, when using ceramic capacitors in small packages—indeed, when using any component—it is extremely important to read the data sheet. Regrettably, often the commonly available data sheets are abbreviated and will provide little of the information you'll need to make an informed decision, so you may have to press the manufacturer for more details.

What about those Y5Vs that I summarily rejected? For kicks, let's examine a common Y5V capacitor. I chose a 4.7-µF, 0603-packaged capacitor rated at 6.3V—I won't mention the vendor, because its Y5V cap is no worse than any other vendor's Y5V cap—and looked at the specs at 5V and +85°C. At 5V, the typical capacitance is 92.9% below nominal, or 0.33 µF.

That's right. Biasing this 6.3V-rated capacitor with 5V will result in a capacitance that is 14 times smaller than nominal.

At +85°C with 0V bias, the capacitance decreases by 68.14%, from 4.7 to 1.5 µF. Now, you might expect this to reduce the capacitance under 5V bias from 0.33 to 0.11 µF. Fortunately, however, those two effects do not combine in this way. In this particular case, the change in capacitance with 5V bias is worse at room temperature than at +85°C.

To be clear, with this part under 0V bias, the capacitance drops from 4.7 µF at room temperature to 1.5 µF at +85°C, whereas under 5V bias the capacitance increases with temperature, from 0.33 µF at room temperature to 0.39 µF at +85°C. This result should convince you that you really need to check component specifications carefully.

GETTING DOWN TO SPECIFICS

As a result of this lesson, I no longer just specify an X7R or X5R capacitor to colleagues or customers. Instead, I specify specific parts from specific vendors whose data I have checked. I also warn customers to check data when considering alternative vendors in production to ensure that they do not run into the problems I encountered.

The larger lesson here, as you may have surmised, is to read the data sheet, every time, without exception. Ask for detailed data when the data sheet does not contain sufficient information. Remember, too, that the ceramic-capacitor designations X7R, Y5V, and so on imply nothing about voltage coefficients. Engineers must check the data to know, really know, how a specific capacitor will perform under voltage.

Finally, keep in mind that, as we continue to drive madly to smaller and smaller sizes, this is becoming more of an issue every day.EDN

ACKNOWLEDGMENT

The author thanks Chris Burkett, field applications engineer at TDK, for his explanation of why ceramic capacitors of the same nominal type can have widely divergent voltage coefficients.

AUTHOR'S BIOGRAPHY

Mark Fortunato is senior principal member of the technical staff in the Communications and Automotive Solutions Group at Maxim Integrated (San Jose, CA). He has spent much of the past 16 years helping customers tame analog circuitry. Before that, Fortunato worked on products ranging from speech-recognition systems to consumer electronics, millimeter-wave instrumentation, and automated
teller machines. He regrets that he never got to meet Jim Williams or Bob Pease.

Highly resonant wireless power

Late in 2012, Efficient Power Conversion (EPC) made available a demonstration board, or more correctly a suite of boards, that act as a demonstrator and development tool for a wireless power transfer scheme. EPC is a maker of gallium nitride power transistors, and the wireless power application is one vehicle the company employs to make the case for using GaN devices where a combination of high frequency, voltage and power is required. This short article is not so much a tear-down – no tearing down is needed, the boards are a development tool, not a packaged product - more an overview of the elements needed to assemble a wireless power transfer system.

Many existing solutions for wireless power transfer use relatively low frequencies, typically 100 to 300 kHz – effectively, transferring power purely via magnetic coupling. This board set uses the architecture devised by WiTricity, which licenses intellectual property to product developers; which operates at a much higher frequency, with highly-resonant coupled coils. WiTricity believes this approach is capable – among other advantages – of transferring power without excessive losses over much greater distances.

EPC's EPC9104 Highly Resonant Wireless Power Transfer system (Figure 1) is capable of delivering 15W DC to a load from 24 VDC input to the source. It consists of [A] an amplifier switching at 6.78 MHz, a source resonator [B] with impedance matching network, a capture resonator [C] with impedance matching network, and rectifier with high frequency filtering [D]. 6.78 MHz is an attractive operating frequency for wireless power transfer as it enables the power transfer coils to be fabricated as extremely thin printed circuits so they can be integrated into mobile devices. 6.78 MHz happens to be the lowest non licensed frequency band available designated for industrial, scientific, and medical (ISM) equipment, and is an excellent choice for many wireless power transfer applications.

One challenge for such wireless technology is efficient power transfer across a significant distance between the source and capture resonators. Highly resonant, impedance matched circuits on both the source and capture devices provide the highest possible coil to coil efficiency. In order to maximise the total efficiency of a wireless power transfer system, the designer must also seek to minimise switching losses of the amplifier that drives the source resonator. At high switching frequencies such as 6.78 MHz, EPC eGaN FETs deliver the required efficiency. The EPC9104 delivers 15W across one inch of air at over 70% end-to-end efficiency. The primary configuration of the demo is open-loop so VOUT varies with VIN as shown in Figure 2. Underneath the heatsink on the amplifier, we find the "power plant" of the system shown in Figure 3. It features the EPC2014 in a half-bridge configuration (Q40 and Q41) driven by the LM5113 half bridge driver for enhancement mode GaN FETs from Texas Instruments (U20). The EPC2014 is a 40-V, 16-mΩ (maximum @ VGS = 5V), eGaN FET. Critical specifications are shown in Table 1. The key to the efficiency performance is the ultra-low RDS(ON) x QG and RDS(ON) x QGD Figures of Merit (FOMs), and low RDS(ON) x QOSS FOM, along with the low inductance of the 1.7 x 1.1 mm wafer-level package. Two challenges that face the power switches in this application are low threshold and limited VGS overhead. The LM5113 is ideally suited to driving the eGaN FETs because it has a low impedance turn off, separate turn on and turn off pins, bootstrap clamp, minimal and matched

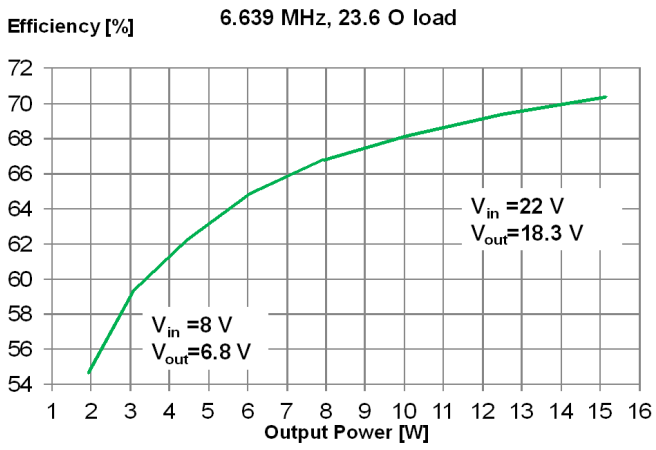
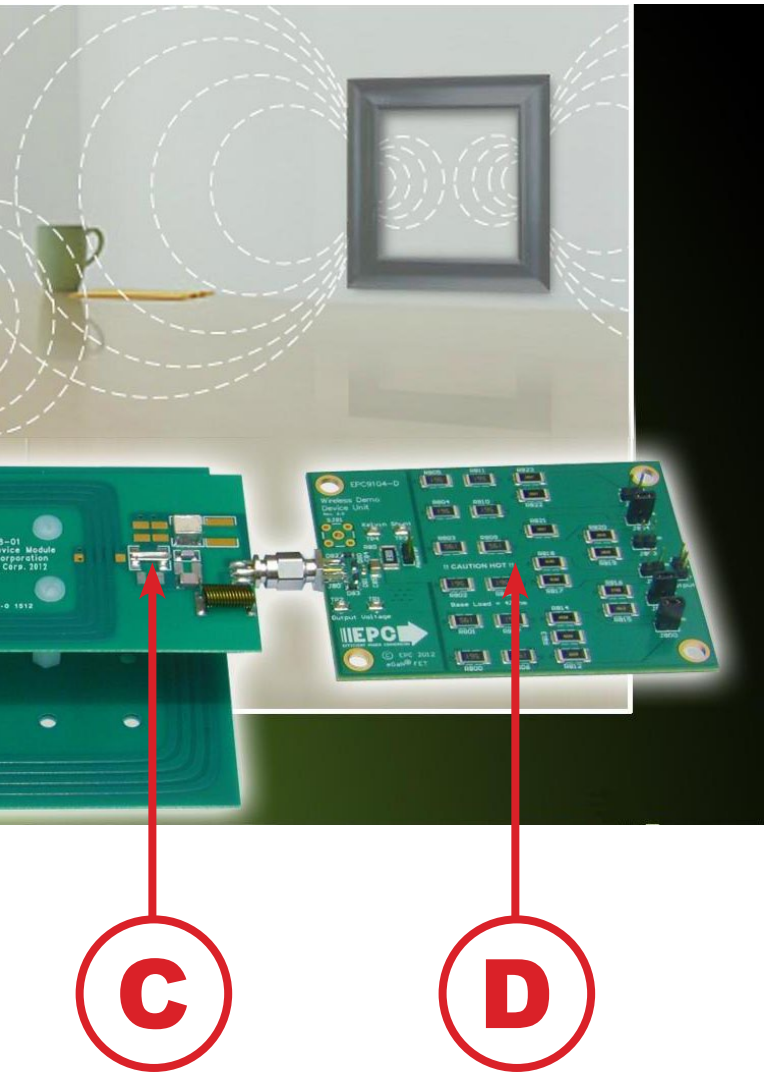


Figure 2 System efficiency plotted against total power delivered over the link.

transfer system teardown

propagation delay and most importantly, greater than 50 V/nsec dv/dt capability. The 2 x 2 mm micro SMD package allows efficient, common heat sinking of all power devices.
Supporting the power plant are two Microchip low dropout regulators, MCP1703 5 MC in the 2 x 3 mm DFN package, chosen for the small size. The demo is quite flexible and allows the user to free run or synchronise to an external oscillator, and run open-loop or close it for a controlled output (using external circuitry). For self free running operation, the source board uses a CB3-3C-7M3728, 7.3728 MHz crystal oscillator to start up the system. Closing the loop requires a precision reference and ultrafast precision comparator. The LM4125AIM5-2.5 is a precision, low power low dropout reference from Texas Instruments. The comparator is a LT1016CS8, 10 nsec comparator capable of being run from a single 5V supply.



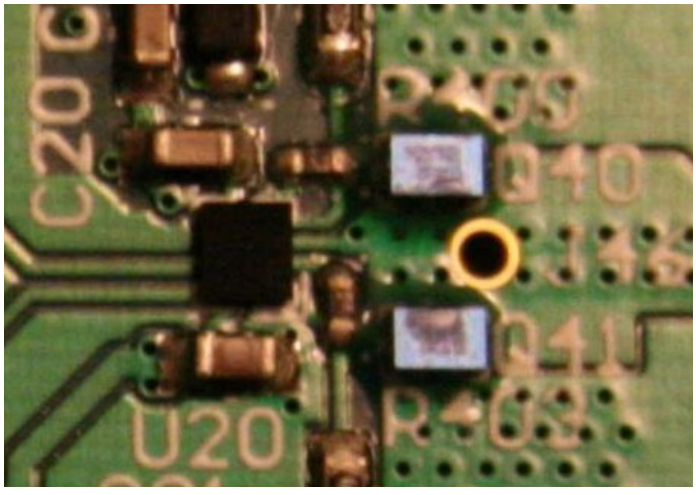


Figure 3 The driver stage that produces the RF power waveform.

THE EPC9104 DELIVERS 15W ACROSS ONE INCH OF AIR AT OVER 70% END-TO-END EFFICIENCY

The source and capture resonators are provided by WiTricity Corporation. These are high Q resonant circuits that are tuned to 6.78 MHz to maximise power transfer efficiency over distance, even when the magnetic coupling factor is low. Note that commercialisation of products using highly resonant wireless power transfer requires a license from WiTricity to its patent portfolio.
The device board [D] consists of a simple rectifier bridge of PD3S140, 40-V Schottky rectifiers from Diodes, Inc. The rectifier is loaded by an array of jumper selectable resistor loads.
Efficient Power Conversion, www.epc-co.com
WiTricity, www.witricity.com

V_{DS}	Abs. Max.	40 V
$V_{GS(TH)}$	V_{DS} = V_{GS} = 2 mA	1.4 V (typ)
$R_{DS(ON)}$	V_{GS} = 5 V, I_D = 10 A	16 mΩ (max)
Q_G	V_{DS} = 20 V, V_{GS} = 5 V I_D = 10 A	2.48 nC (typ)
Q_{GD}	V_{DS} = 20 V, I_D = 10 A	0.48 nC
Q_{GS}		0.67 nC
Q_{OSS}	V_{DS} = 20 V, V_{GS} = 0 V	4.8 nC

Table 1 EPC2014 device key parameters

DETECTING AND DISTINGUISHING CARDIAC-PACING ARTIFACTS

IMAGE: ISTOCK

BURIED IN NOISE AND LARGER CARDIAC SIGNALS, THE ARTIFACTS OF A PACEMAKER ARE DIFFICULT TO SPOT. THE METHODOLOGY PRESENTED HERE CAN HELP DIAGNOSTICIANS READ BETWEEN THE LINES OF AN ECG STRIP.

JOHN KRUSE AND CATHERINE REDMOND • ANALOG DEVICES INC

When a heart patient with an implanted pacemaker undergoes electrocardiogram testing, the cardiologist must be able to detect the presence and effects of the pacemaker (see sidebar, "When the heart's electrical subsystem malfunctions". A simple implanted pacer's activity is generally not perceptible on a normal ECG trace, because the very fast pulses—with typical widths of hundreds of microseconds—get filtered due to low-bandwidth display resolution (monitor/diagnostic 40-/150-Hz bandwidths). The pacer's signal, however, can be inferred through the changed morphology of the ECG trace, which is representative of the heart's own electrical activity as recorded at the skin surface via ECG leads.

It is important to be able to detect and identify pacing artifacts because they indicate the presence of the pacemaker and help in evaluating its interaction with the heart. But the artifacts' small amplitude, narrow width, and varying waveshape make them difficult to detect, especially in the presence of electrical noise that can be many times their amplitude. At the same time, pacing therapy has become extremely advanced, with dozens of pacing modes available for single- to three-chamber pacing. Complicating the detection of pacing artifacts, pacemakers produce lead-integrity pulses, minute-ventilation (MV) pulses, telemetry signals, and other signals that can be incorrectly identified as pacing artifacts.

The use of real-time pacemaker telemetry has made the display of pacing artifacts on an ECG strip less important than it used to be. An individual skilled in pacing therapies can look at the strip and sometimes infer the type of pacing therapy being administered to the patient and determine whether the pacemaker is working properly.

In addition, all pertinent medical standards require the display of pacing artifacts, though they vary somewhat in their specific requirements for the height and width of the captured pacer signal. The applicable standards include Association for the Advancement of Medical Instrumentation (AAMI) specifications EC11:1991/(R)2001/(R)2007 and EC13:2002/(R)2007, as well as International Electrotechnical Commission specifications IEC 60601-1 ed. 3.0b:2005, IEC 60601-2-25 ed. 1.0b, IEC 60601-2-27 ed. 2.0:2005, and IEC 60601-2-51 ed. 1.0:2005.

HOW PACEMAKERS PACE

Implantable pacemakers (Figure 1) are typically lightweight and compact. They contain the circuitry necessary to monitor the heart's electrical activity through implanted leads and to stimulate the heart muscle as necessary to ensure a regular heartbeat. Pacemakers must be low-power devices, as they operate with a small battery that typically has a 10-year lifespan. The National Academy of Engineering estimated in 2010 that more than 400,000 pacemakers are implanted in patients every year (Reference 1).

AT A GLANCE

- A simple implanted pacer's activity is generally not perceptible on a normal ECG trace, because the very fast pulses get filtered out. Individuals skilled in pacing therapies, however, can examine the ECG trace to confirm the presence of a pacemaker and evaluate its interaction with the heart.
- Artifacts from implanted pacemakers can vary from 2 to 700 mV, with durations between 0.1 and 2 msec and rise times between 15 and 100 µsec. The presence of electrical noise that can be many times their amplitude makes the pacing artifacts difficult to detect.
- A major noise source is the H-field telemetry scheme used by most implantable heart devices.
- The ADAS1000 ECG analog front end embeds an algorithm that can help distinguish pacing artifacts and display them on the ECG strip chart.

In unipolar pacing, the pacing leads consist of an electrode at the tip of a single pacing lead and the metal wall of the pacemaker housing itself. The pacing artifacts caused by this mode of pacing can be several hundred millivolts at the skin surface, with a width of up to 2 msec. Unipolar pacing is no longer commonly used, however.

In bipolar pacing, which today accounts for the bulk of pacing artifacts created, the heart is paced from the electrode at the tip of the pacing lead. The return electrode is a ring electrode located very close to the tip electrode. The artifacts that this type of lead produces are much smaller than those produced by unipolar pacing; pulses on the skin surface can be as small as a few hundred microvolts high and 25 µsec wide, with average artifacts measuring 1 mV high and 500 µsec wide. The amplitude of the artifact can be much smaller when the detection vector does not line up directly with the pacing lead vector.

Many pacemakers can be programmed for pulse widths as short as 25 µsec, but the short-pulse-width settings are typically used only in pacemaker threshold tests performed in an electrophysiology laboratory. Setting the lower limit to 100 µsec eliminates the problem of falsely detecting MV and lead-integrity (LV lead) pulses as valid pacing artifacts. These subthreshold pulses are usually programmed to be between 10 and 50 µsec.

Various types of pacemakers are available for pacing specific chambers of the heart. Single-chamber pacing delivers pacing therapy to either the right atrium or the right ventricle. Such a pacer can be either unipolar or bipolar. Dual-chamber pacing delivers pacing therapy to both the right atrium and the right ventricle. Biventricular pacing delivers pacing therapy to both the right ventricle and the left ventricle; in addition, the heart is usually paced in the right atrium.

The biventricular pacing mode can be difficult to display properly, for two main reasons. First, the two ventricle paces may occur at the same time, appearing as a single pulse at the skin surface. Second, the left-ventricle lead placement is generally not on the same vector as the right-ventricle lead and may actually be orthogonal to it. Usually, the right atrium is best displayed in lead aVF—one of the augmented limb

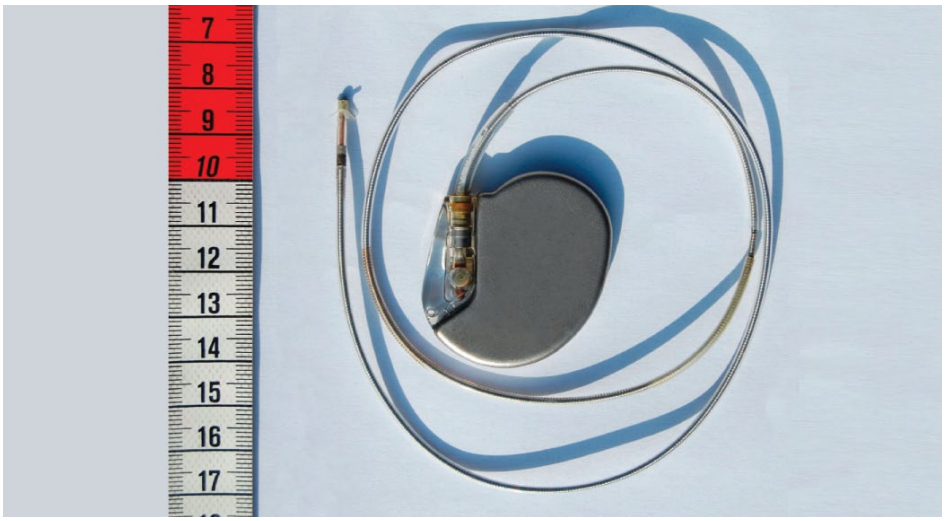


Figure 1 Pacemakers must be light, compact, low-power devices (Reference 2).

leads—and the right ventricle is best displayed in lead II. Most ECG systems do not employ three simultaneous lead-detection circuits or algorithms, making the left ventricle the toughest lead to pick up. Thus, it is sometimes best detected in one of the V leads.

ARTIFACT WAVEFORMS

Most pacing pulses have very fast rising edges. The rise time measured at the pacemaker output is generally about 100 nsec. When measured at the skin surface, the rise time will be slightly slower because of the inductance and capacitance of the pacing lead. Most pacing artifacts at the skin surface are on the order of 10 µsec or less. As complex devices with built-in protection, pacemakers can produce high-speed glitches that do not affect the heart but do affect pacemaker-detection circuits.

Figure 2 shows an example of an ideal pacing artifact. The positive pulse has a fast rising edge. After the pulse reaches its maximum amplitude, a capacitive droop follows, and then the trailing edge occurs. The artifact next changes polarity for the recharge portion of the pacing pulse. The recharge pulse is required so that the heart tissue is left with a net-zero charge; with a monophasic pulse, ions would build up around the electrodes, creating a dc charge that could lead to necropsy of the heart tissue.

Introducing cardiac-resynchronization devices adds another degree of complication in detecting and displaying pacing artifacts. These devices pace the patient in the right atrium and both ventricles. The pulses in the two ventricles can fall close together, overlap, or occur at exactly the same time; the left ventricle can even be paced before the right ventricle. Currently, most devices pace both ventricles at the same time, but studies have shown that adjusting the timing will benefit some patients by yielding a higher cardiac output.

Detecting and displaying both pulses separately is not always possible, and many times the pulses will appear as a single pulse on the ECG electrodes. If both pulses were to occur at the same time with the leads oriented in opposite directions, the pulses could cancel each other out on the skin surface. The probability of such an occurrence is remote, but one can envision the appearance on the skin surface of two ventricle-pacing artifacts with opposite polarities. If the two pulses were offset by a small time interval, the resulting pulse shape might be very complex.

Figure 3 shows scope traces of a cardiac-resynchronization device pacing in a saline tank. This is a standard test environment for pacemaker validation, designed to mimic the conductivity of the human body. The proximity of the scope probes to the pacing leads causes the amplitudes to be much larger than what would be expected on the skin surface, however, and the low impedance that the saline solution presents to the ECG electrodes results in much less noise than would normally be seen in a skin-surface measurement.

The first, second, and third pulses shown in the figure (l to r) are the atrial, right-ventricle, and left-ventricle pulses, respectively. The leads were placed in the saline tank with vectors optimized to see the pulses clearly. The negative-going pulse is the pace; the positive-going pulse is the recharge. The amplitude of the atrial pulse is slightly larger than the two other pulse amplitudes because the lead was in a slightly better vector than the ventricle leads; in actuality, all three pacing outputs in the resynchronization device were programmed to have the same amplitude and width. With real patients, the amplitudes and widths are often different for each pacemaker lead.

PACING ARTIFACTS' SMALL AMPLITUDE, NARROW WIDTH, AND VARYING WAVESHAPES MAKE THEM DIFFICULT TO DETECT.

ARTIFACT DETECTION

It is impossible to detect all pacing artifacts and reject all possible noise sources in a cost-effective manner. Among the challenges are the number of chambers that the pace detection must monitor, the interference signals encountered, and the wide variety of pacemakers in use. Solutions for detecting artifacts may range from hardware implementations to digital algorithms.

The pacing leads for cardiac-resynchronization devices will not all have the same vector. The right-atrium lead usually aligns with lead II, but it can sometimes point straight out of the chest, so a Vx (precordial lead) vector may be needed to see it. The right-ventricle lead is usually placed at the apex of the right ventricle, so it usually aligns well with lead II. The left-ventricle pacing lead, threaded through the coronary sinus, is actually on the outside of the left ventricle. This lead usually aligns with lead II but may have a V-axis orientation.

The pacing leads of implantable defibrillators and resynchronization devices are sometimes placed in areas of the heart that have not had an infarction. Placing them around infarcts is the main reason that this system uses three vectors and requires a high-performance pacing-artifact detection function.

A major noise source is the H-field telemetry scheme used in most implantable heart devices. Other sources of noise are transthoracic-impedance measurements for respiration, electric cautery, and conducted noise from other medical devices connected to the patient.

Complicating the problem of acquiring pacing artifacts, each pacemaker manufacturer uses a different telemetry scheme. In some cases, a single manufacturer may use different telemetry systems for different implantable-device models. Many implantable devices can communicate using both H-field telemetry and either ISM- or Medical Implant Communication Service (MICS)-band telemetry. The variability of H-field telemetry from one model to the next makes filter design difficult. ECG devices have to be Class CF—the most stringent classification—as there is direct conductive contact with the heart, whereas other medical devices may be built to less stringent Class B or BF requirements, and their higher leakage currents may interfere with the performance of ECG-acquisition devices.

ARTIFACT-DETECTING AFE

The ADAS1000 (Figure 4) is a five-channel analog front end designed to

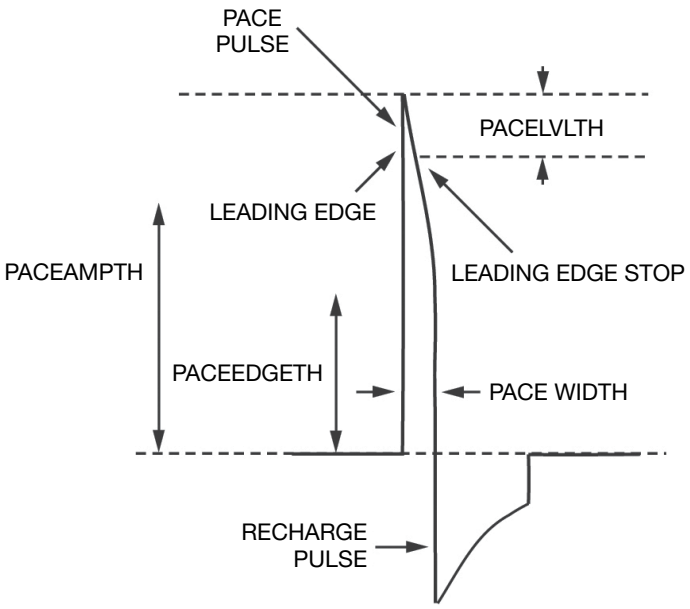


Figure 2 In this example of an ideal pacing artifact, the positive pulse has a fast rising edge. After the pulse reaches its maximum amplitude, a capacitive droop follows, and then the trailing edge occurs. The artifact then changes polarity for the recharge portion of the pacing pulse.

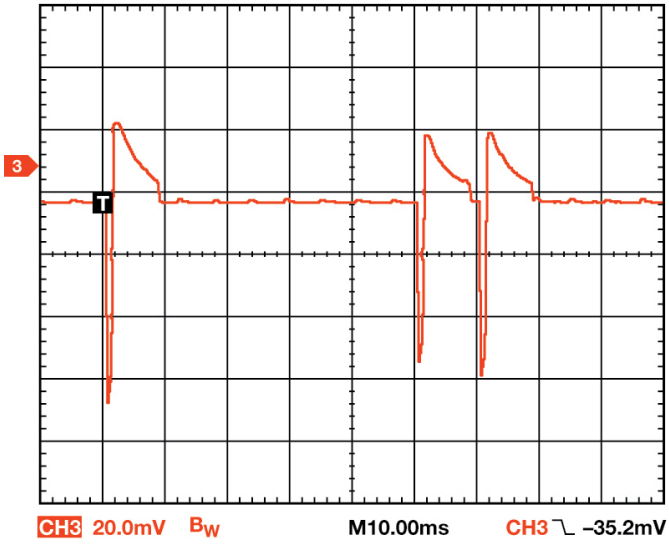


Figure 3 Scope traces are shown for a cardiac-resynchronization device pacing in a saline tank—a standard test environment for pacemaker validation.

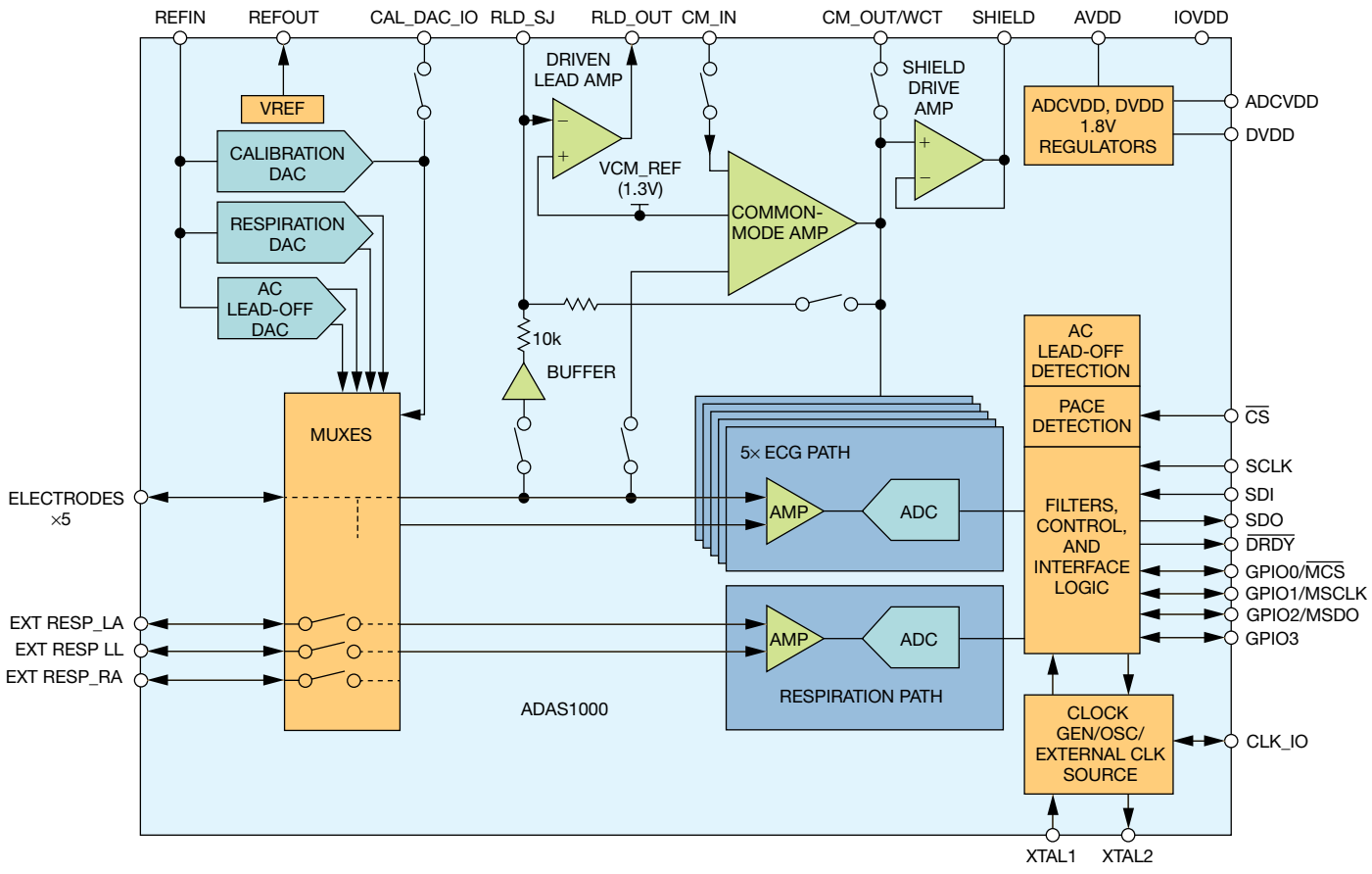


Figure 4 The block diagram shows the ADAS1000 analog front end.

When the heart's electrical subsystem malfunctions

The heart, a biochemical-electromechanical system, develops an electrical impulse that travels from the sinoatrial (SA) node in the upper right atrium to the atrioventricular (AV) node. The SA node acts as the pacemaker for the system (Figure 1).
This electrical impulse generates the P wave, which can be seen on the ECG capture in Figure 2. From the AV node, the electrical signal propagates, via the His-Purkinje system, to the ventricles, causing the ventricle muscles to contract. Their contraction (the R wave) moves oxygenated blood from the left ventricle into and through the body, and moves deoxygenated blood from the right ventricle to the lungs.
When the electrical system doesn't work perfectly, different heart conditions can occur. For example, bradycardia occurs when the heart beats too slowly or misses beats. A typical surgical intervention for this condition would be to implant a pacemaker device (pulse generator) just under the skin of the patient's chest, with endocardial leads routed through the veins directly to the heart, as shown in Figure 3.
In another class of arrhythmias, called tachycardia, the heart beats too fast. This very serious condition is treated with implantable cardiac defibrillators (ICDs). Modern ICDs can also treat many bradycardia arrhythmias.
Heart failure can occur when the heart becomes enlarged, lengthening its conduction paths and upsetting the timing of the ventricular contractions. This forms a positive feedback system, further aggravating the heart. Implantable cardiac resynchronization (ICR) devices retime the ventricles by pacing both ventricles and usually one atrium. These devices improve cardiac output, allowing the heart to recover to a certain degree. Cardiac resynchronization therapy (CRT) devices include an ICD as part of the system.

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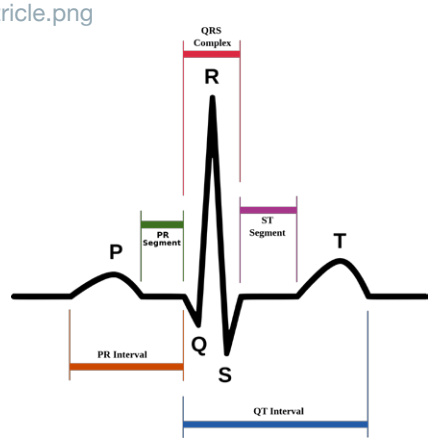

Figure 2 Electrical action during heart-muscle contractions (Reference 2).

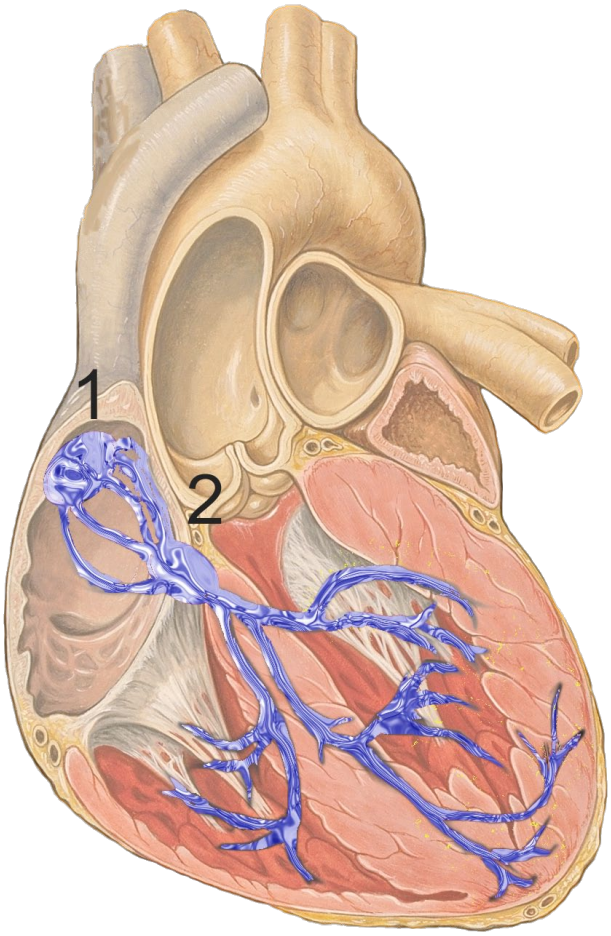

Figure 1 The heart muscle showing sinoatrial (1) and atrioventricular (2) nodes. (Reference 1).

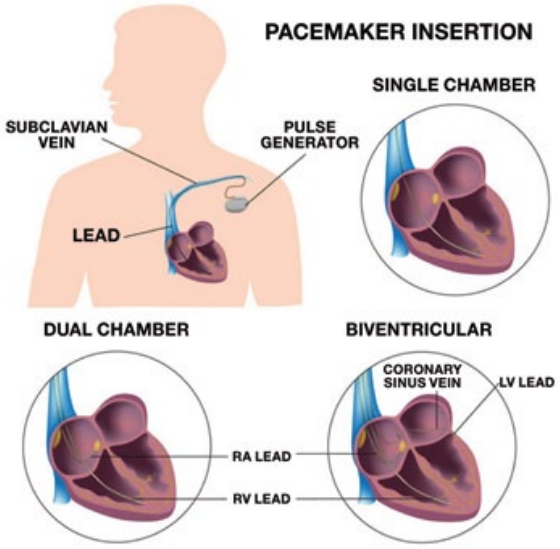

Figure 3 Pacemaker-lead insertions for the various pacemaker types. (RA is right atrium, RV is the right ventricle; LV is the left ventricle).

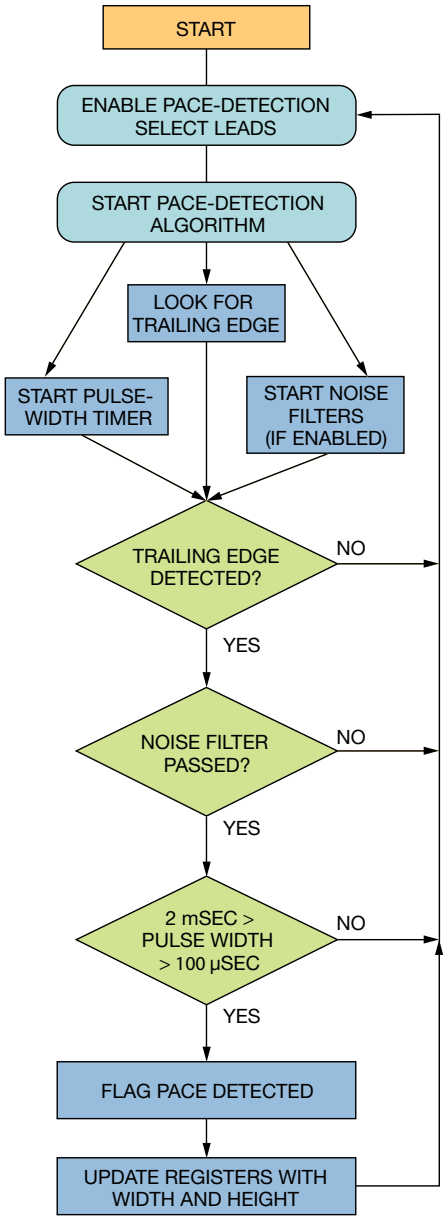

Figure 5 The flowchart shows the digital-pacemaker decision process for the artifact-detection algorithm, which detects pacing artifacts with widths that range from 100 µsec to 2 msec and amplitudes that range from 400 µV to 1000 mV.

address some of the challenges facing designers of low-power, low-noise, high-performance, tethered or portable ECG systems. The AFE, designed for both monitor- and diagnostic-quality ECG measurements, comprises five electrode inputs and a dedicated right-leg-drive (RLD) output reference electrode. In addition to supporting the essential ECG signal-monitoring elements, the AFE enables such functions as respiration (thoracic impedance) measurement, lead/electrode connection status, internal calibration, and capabilities for pacing-artifact detection.

One ADAS1000 supports five electrode inputs, facilitating a traditional, six-lead ECG measurement. By cascading a companion ADAS1000-2 device, the system can be scaled up to a true 12-lead measurement; by cascading three or more devices, the system can be scaled to measurements with 15 leads and beyond.

DETECTION ALGORITHM

The device's front end includes a digital pacemaker artifact-detection algorithm that detects pacing artifacts with widths ranging from 100 µsec to 2 msec and amplitudes ranging from 400 µV to 1000 mV, to align with AAMI and IEC standards. Figure 5 is a flow diagram of the algorithm.

The pace-detection algorithm runs three instances of a digital algorithm on three of four possible leads (I, II, III, or aVF). It runs on the high-frequency ECG data, in parallel with the internal decimation and filtering, and returns a flag that indicates pacing was detected on one or more of the leads, providing the measured height and width of the detected signal. For users who wish to run their own digital pace algorithm, the ADAS1000 supplies a high-speed pace interface that provides the ECG data at a 128-kHz data rate; the filtered and decimated ECG data remains unchanged on the standard interface.

A minute-ventilation filter is built into the ADAS1000 algorithm. MV pulses, which are conducted from the ring of a bipolar lead to the housing of the pacemaker, detect respiration rates to control the pacing rate. They're always less than 100 µsec wide, varying from about 15 to 100 µsec.

The simultaneous three-vector pacing-artifact system can detect pacing artifacts in noisy environments. Each of the three instances of the pace algorithm can be programmed to detect pace signals on different leads (I, II, III, or aVF). Programmable threshold levels tailor the algorithm to detect the range of pulse widths and heights presented, with internal digital filters designed to reject heartbeat, noise, and MV pulses. When a pace has been validated in an individual instance of the pace signal, the device outputs a flag so that the user can mark or identify the pace signal in the ECG capture strip.

The choice of sample rate for the pacing-artifact algorithm is significant because it cannot be exactly the same frequency as those used for the H-field telemetry carrier by the three pacing-systems companies (Boston Scientific, Medtronic, and St Jude). All three vendors use different frequencies, and each has many different telemetry systems. Analog Devices believes that the ADAS1000's sampling frequency does not line up with that of any of the major telemetry systems. EDN

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BY JERAD LEWIS • ANALOG DEVICES INC

Common inter-IC digital interfaces for audio data transfer

UNDERSTANDING THE PROS AND CONS OF DIFFERENT INTERFACES BEFORE SELECTING PARTS HELPS TO STREAMLINE YOUR COMPONENT SELECTION AND ENSURE THAT YOU HAVE THE MOST EFFICIENT IMPLEMENTATION OF THE SIGNAL CHAIN.

As audio integrated circuits move to finer geometries, it becomes more difficult to design—and less cost-effective to integrate—high-performance analog circuits on the same piece of silicon with high-density digital circuits. Audio-system architects thus are pushing analog portions of the audio signal chain further toward the input and output transducers and are connecting everything in between digitally.

A traditional audio signal chain may have analog signal connections between microphones, preamps, ADCs, DACs, output amplifiers, and speakers, as shown in Figure 1. As the analog circuits are pushed to the edges of the signal chain, however, digital interfaces between ICs in the chain become more prevalent. DSPs have always had digital connections, but now digital interfaces are being included on the transducers and amplifiers, which typically have had only analog interfaces.

IC designers are integrating ADCs, DACs, and modulators in the transducers on opposite ends of the signal chain, thereby eliminating the need to route any analog audio signals on the PCB, as well as reducing the number of devices in the signal chain. Figure 2 shows an example of a completely digital audio signal chain.

Many standards exist for transmitting digital audio data. Some formats, such as I²S (inter-IC sound), TDM (time-division multiplexed), and PDM (pulse-division multiplexed), are typically used to enable inter-IC communication on the same PCB. Other formats, such as S/PDIF and Ethernet AVB, primarily target data connections from one PCB to another through cabling.

This article focuses on the differences, advantages, and disadvantages of the inter-IC digital audio formats. Choosing audio components with mismatched digital interfaces needlessly complicates the system design. Understanding the pros and cons of the different interfaces before selecting parts helps to streamline component selection and ensure the most efficient implementation of the signal chain.

Inter-IC Sound (more commonly called “I squared S” or “I two S”) is the most common digital audio format used for audio data transfer between ICs. Philips Semiconductors—now NXP—introduced the I²S standard in 1986; the format was revised in 1996. The interface was first popularly used in CD-player designs and now can be found in almost any application that involves the transfer of digital audio data from one IC to another. Most audio ADCs, DACs, DSPs, and sample-rate converters, as well as some microcontrollers, include I²S interfaces.

An I²S bus uses three signal lines for data transfer: a frame clock, a bit clock, and a data line. The receiving IC, the transmitting IC, or even a separate clock-master IC can generate the two clocks, depending on the system architecture (Figure 3). An IC with an I²S port often can be set to be in either master or slave mode. Unless the design uses a sample-rate converter in the signal chain, a system will usually have a single I²S master device so that there are no issues with data synchronization.

The Philips standard for these signals uses the designations WS for word select, SCK for the clock, and SD for the data, although IC manufacturers seem to use those names only rarely in their IC data sheets. Word select is also commonly called LRCLK, for “left/right clock,” and SCK may

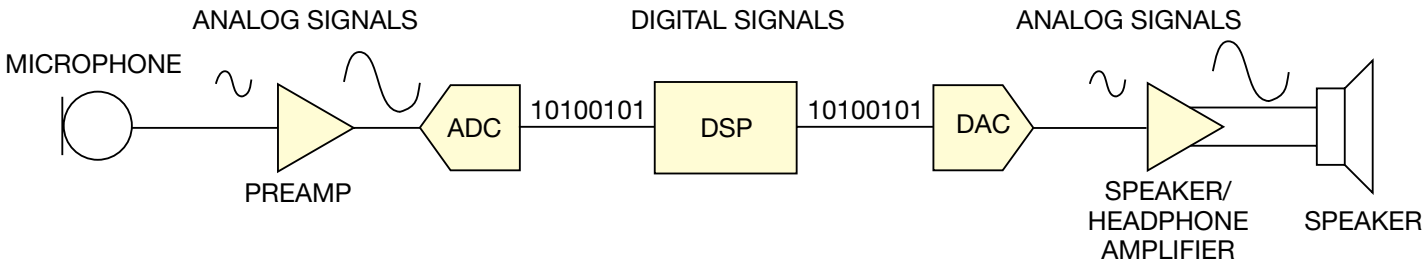

Figure 1 A traditional audio signal chain may have analog signal connections between microphones, preamps, ADCs, DACs, output amplifiers, and speakers.

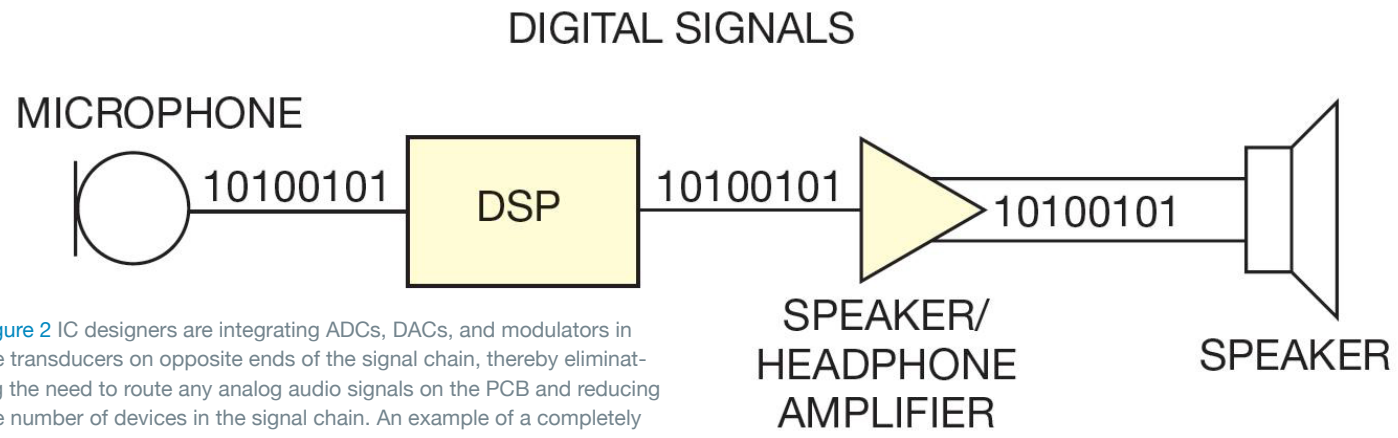

Figure 2 IC designers are integrating ADCs, DACs, and modulators in the transducers on opposite ends of the signal chain, thereby eliminating the need to route any analog audio signals on the PCB and reducing the number of devices in the signal chain. An example of a completely digital audio signal chain is shown here.

alternatively be called BCLK, for "bit clock," or SCLK, for "serial clock."

The name of an IC's serial data pin varies most from one IC vendor to another and even among a single vendor's products. A quick survey of audio IC data sheets shows that the SD signal may also be called SDATA, SDIN, SDOUT, DACDAT, ADCDAT, or other variations on these, depending on whether the data pin is an input or an output.

An I²S data stream can carry one or two channels of data with a typical bit-clock rate between 512 kHz, for an 8-kHz sampling rate, and 12.288 MHz, for a 192-kHz sampling rate. The data word length is often 16, 24, or 32 bits. For word lengths less than 32 bits, the frame length is often still 64 bits; the unused bits are just driven low by the transmitting IC.

Although it is rare, some ICs support only I²S interfaces with a maximum of 32- or 48-bit clocks per stereo-audio frame. When using such an IC, the system designer must take care to ensure that the devices on the other end of its connections also support those bit-clock rates.

Though I²S is the most commonly used format, there are other variants of the same three-wire configuration, such as left-justified, right-justified, and PCM modes. Such formats differ from I²S based on the position of the data word in the frame, the polarity of the clocks, or the number of bit-clock cycles in each frame.

TDM FORMATS

Some ICs support multiple I²S data inputs or outputs using a common clock, but such an approach obviously increases the number of pins necessary to transfer the data. TDM formats are used when more than two channels of data are to be transferred on a single data line. A TDM data stream can carry as many as 16 channels of data and has a data/clock configuration similar to that of I²S.

Each channel of data uses a slot on the data bus that is 1/Nth the width of the frame, where N is the number of channels being transferred. For practical purposes, N is usually rounded up to the nearest power of two (2, 4, 8, or 16), and any additional channels are left empty. A TDM frame clock is often implemented as a single bit-wide pulse, as opposed to the 50% duty-cycle clock of I²S. Clock rates above 25 MHz are not commonly used for TDM data, because higher frequencies cause board-layout issues that PCB designers would rather avoid.

TDM is commonly used for systems in which multiple sources feed one input or one source drives multiple devices. In the former case (multiple sources feeding one input), each TDM source shares a common data bus. The source must be configured to drive the bus only during its appropriate channel and to tristate its driver when other devices are driving other channels.

No standard akin to the Philips standard for I²S exists for TDM interfaces, and as a result many ICs have their own, slightly different flavor of TDM implementation. The variants can differ in such aspects as clock polarity, channel configuration, and tristating or driving unused channels. Of course, the different ICs will usually work together, but the system

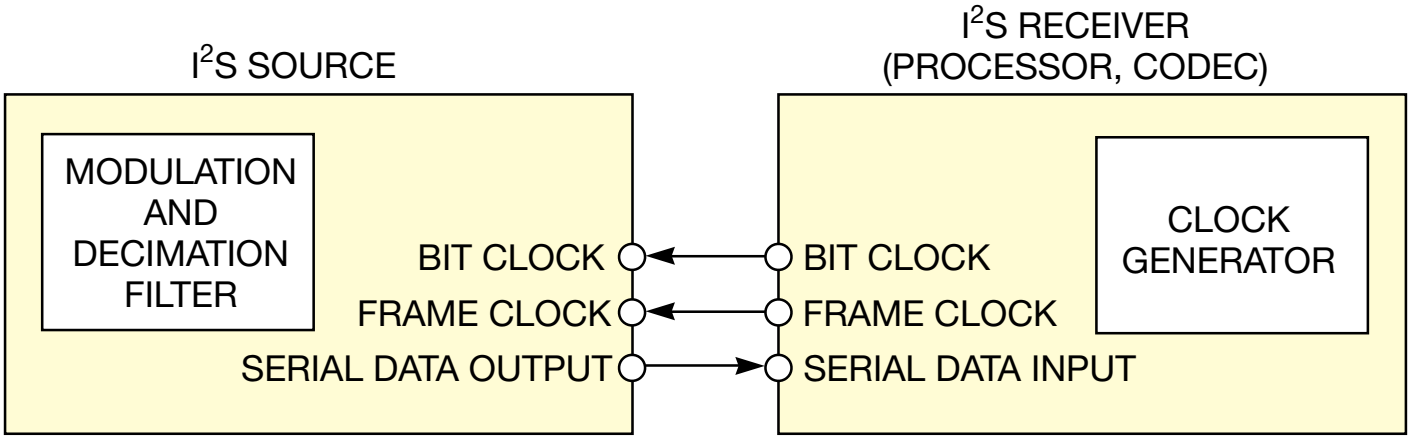

Figure 3 An I²S bus uses three signal lines for data transfer: a frame clock, a bit clock, and a data line. The receiving IC, the transmitting IC, or even a separate clock-master IC can generate the two clocks, depending on the system architecture.

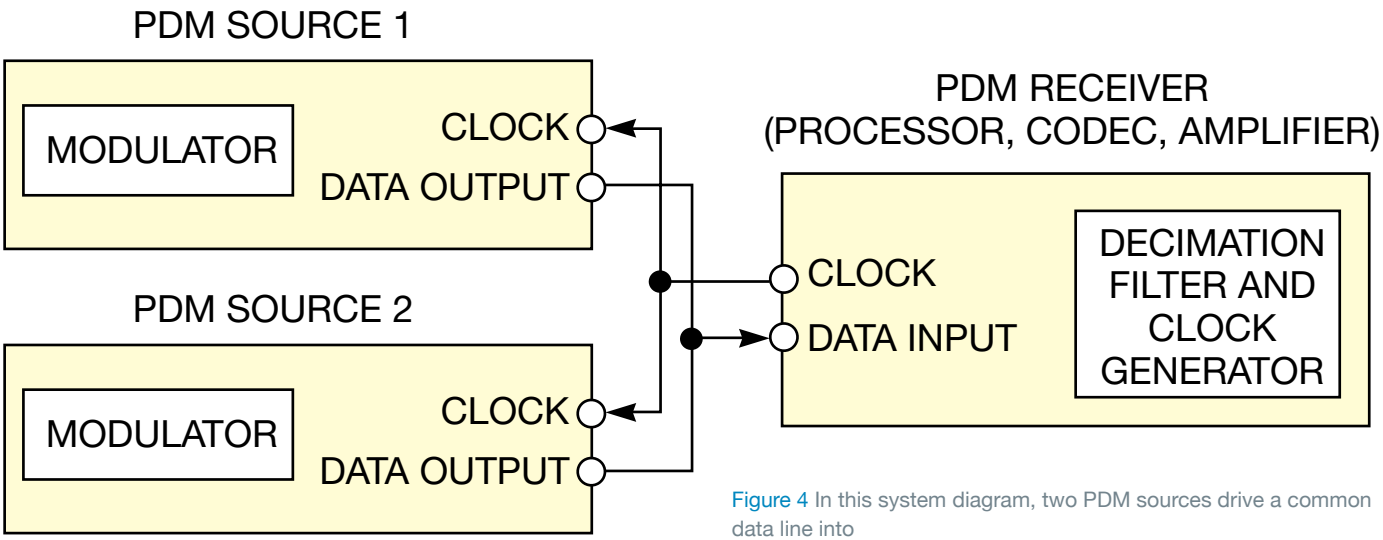

Figure 4 In this system diagram, two PDM sources drive a common data line into a receiver.

designer must take care to ensure that the outputs of one device will will output data in the format that the inputs of another are expecting.

PDM DATA CONNECTIONS

PDM data connections are becoming more common in portable audio applications, such as cell phones and tablet computers. PDM is an advantage in size-constrained applications because it allows audio signals to be routed around noisy circuitry, such as LCD screens, without having to deal with the interference issues that analog audio signals may have.

With PDM, up to two audio channels can be transmitted with only two signal lines. Figure 4 shows a system diagram with two PDM sources driving a common data line into a receiver. The system master generates a clock that can be used by two slave devices, which use alternate edges of the clock to output their data on a common signal line.

The data is modulated at a 64× rate, resulting in a clock that is typically between 1 and 3.2 MHz. The bandwidth of the audio signal increases as the clock rate increases, so lower-frequency clocks are used in systems that can trade off a reduced bandwidth for lower power consumption.

A PDM-based architecture differs from I²S and TDM in that the decimation filter is in the receiving IC rather than the transmitting IC. The output of the source is the raw high-sample-rate modulated data, such as the output of a sigma-delta modulator, rather than decimated data, as it is in I²S. A PDM-based architecture reduces the complexity in the source device and often makes use of decimation filters that are already present in a codec's ADCs.

With this approach, system designers not only can use audio codecs that they may already be using but also can take advantage of a digital data connection's reduced sensitivity to interference. Further, decimation filters may be more efficiently implemented in the finer silicon geometries used for fabricating a codec or processor, rather than in the processes used for the microphone ICs.

Codecs, DSPs, and amplifiers have had I²S ports for years, but until now a system's input devices, such as microphones, have had either analog or PDM outputs. As digital interfaces are pushed further toward the ends of the signal chain, new ICs will be needed to support the new system architectures.

Microphones, such as the Analog Devices ADMP441 MEMS microphone, that have an integrated I²S interface make it easier for designers to build this component into systems in which PDM microphones are not easily used or analog interfaces are not desired. Only a subset of audio codecs accepts a PDM input, and very few audio processors outside of those specifically designed for mobile phones and tablets natively accept this type of data stream.

In some designs, an I²S output microphone could completely eliminate the need for any analog front-end circuits because many designs may have only an ADC and PGA to support a microphone input to the processor. An example of such a system is a wireless microphone with a digital transmitter. The wireless transmitter SOC may not have a built-in ADC, so using an I²S output microphone enables completely digital connections between the transducer and transmitter.

I²S, TDM, and PDM audio interfaces each have their advantages and applications for which they are best suited. As more audio ICs transition from analog to digital interfaces, system designers and architects will need to understand which interface would be most appropriate for a particular design. With a digital signal chain from microphone to DSP to amplifier, analog signals can be pushed completely off of the PCB and exist only in the acoustic domain. EDN

ACKNOWLEDGMENT

This article originally appeared on EDN's sister site, Planet Analog, at www.eetimes.com/4374249.

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designideas

READERS SOLVE DESIGN PROBLEMS

An improved offline driver lights an LED string

Yan-Niu Ren, Southwest Petroleum University, Chengdu, China

A constant current is better than a constant voltage for driving LEDs. In this proposed circuit, a common constant-voltage regulator is changed into a constant-current source for LEDs. In addition, a startup current limiter is used to suppress large current surges, and a voltage chopper is employed for a wide ac input of 96 to 260 V_{RMS}.

The concept presented here originates from two Design Ideas published in 2011 (references 1 and 2) and was developed to improve power efficiency at a low cost. The circuits shown in figures 1 and 2 both have the same brilliance of an inductorless chopper and the same controversial issue of power efficiency. To improve the power efficiency, you should observe two principles: The resistors of the chopper should dissipate as little power as possible, and the chopper should switch at the appropriate threshold voltage, V_{TH}. In addition, V_{TH} should be as close as possible to the operating voltage across the LED string. This approach minimizes the power dissipation of the constant-current regulator (CCR) while maintaining a constant LED current.

THIS APPROACH MINIMIZES CCR POWER DISSIPATION WHILE KEEPING LED CURRENT CONSTANT.

The circuit shown in Figure 3 is an example that follows the principles described above, with a power efficiency of about 85%. Voltage regulator IC_1 and R_5 form a 20-mA CCR. The LED string has a sufficient number of LEDs to require 120V at 20 mA. The voltage across R_6 provides a means for indirect measurement of the LED current.

V_{TH} is the diode bridge full-wave rectified output voltage above which, when divided by R_1 to R_3, the 68V bias of D_5 is overcome, turning on Q_1 and turning off Q_2. C_1 charges quickly to V_{TH} while Q_2 is on, then discharges slowly

DIs Inside

39 Low-duty-cycle LED flasher keeps power draw at 4 mW

40 Rotary encoder with absolute readout offers high resolution and low cost

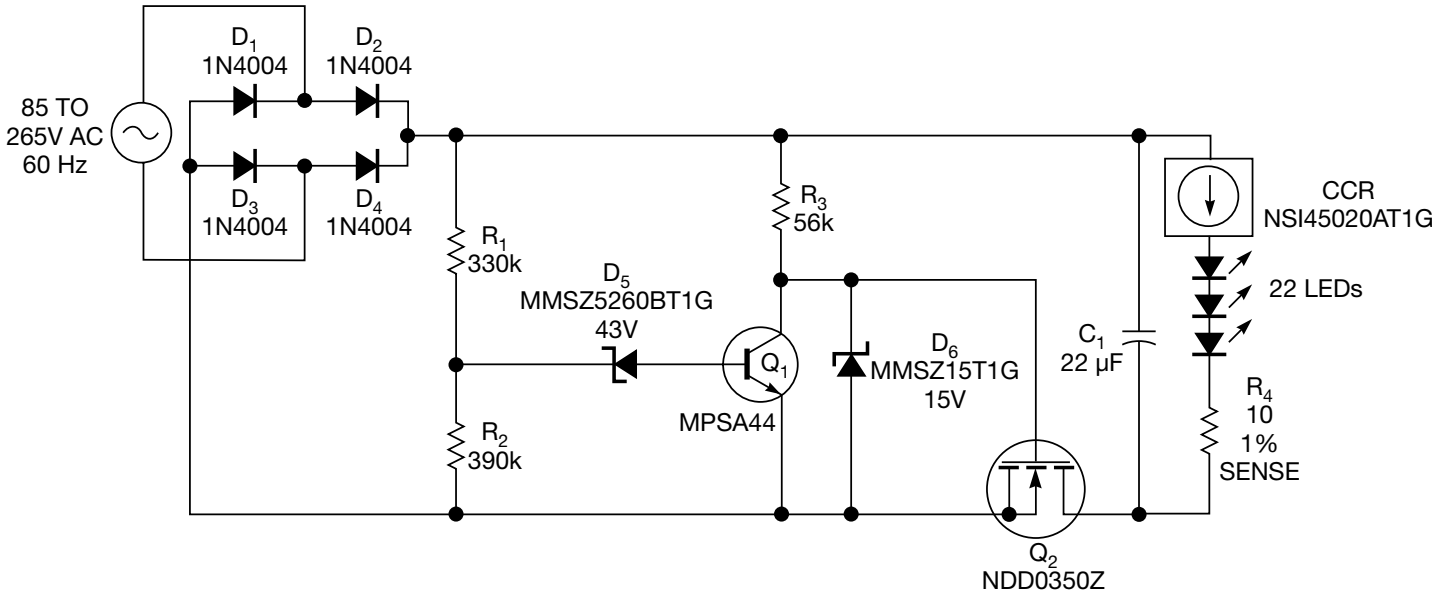


Figure 1 This circuit drives a string of LEDs with a constant current over the entire worldwide range of ac-mains voltages. The resistor in series with the LED string provides a convenient point to measure LED current via its voltage drop.

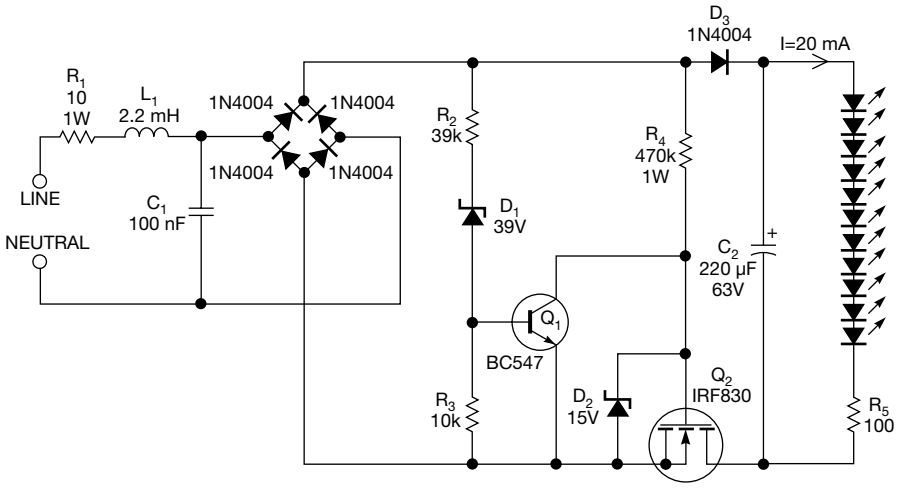


Figure 2 The chopper operation is similar to the circuit of Figure 1; the larger LED series resistor, instead of a constant-current source, provides the current-limit function.

TABLE 1 POWER EFFICIENCY OF IMPROVED CIRCUIT

V_{RMS} ac at 50 Hz	96	140	180	220	260
Power efficiency (%)	90	87	86	85	82

into the LED string until the next half-cycle of the incoming ac.

V_{TH} must be no less than required to maintain the LED operation voltage of 120V at the end of C_1's discharge and no more than 1.414 times the V_{RMS} of the lowest ac level. With 120V required for the LEDs, plus the 3V input-to-output differential required by IC_1, plus 1.25V developed across R_5, the minimum C_1 voltage will be 124.25V. For simplicity, this figure can be rounded up to 125V.

As shown in Figure 4, the C_1 discharge time is much longer than the charge time during a 50-Hz half-cycle of 10 msec. During this period, the peak-to-peak voltage across C_1 is almost 20 mA×10 msec/22 µf=9.09V. Thus, U_{C1_MAX}=125V+9.09V=134.09V. For simplicity, this result can be rounded up to 135V. This is V_{TH}; any voltage above this turns Q_1 on and gets chopped off by Q_2.

When Q_1 switches on, the power consumption of R_4 in Figure 3 is less than 20 mW at 260V_{RMS} input, and the R_1-R_2-R_3-D_5 divider dissipates less than 100 mW. This result is almost negligible compared with the 2.4W consumed by the LEDs. These resistors are large value so as to consume as little power as possible. R_3 allows fine adjustment of V_{TH} to match the actual drop across the LED string.

A startup current limiter has been included to limit the large inrush current surge through C_1 and Q_2 that would occur if the ac were switched on at a time in its cycle just before V_{TH} was reached. A current-limiting resistor would reduce efficiency on every cycle, but R_9 limits only the surge to 1.35A at power-up until C_2 charges sufficiently to turn on Q_3.

As the ac input increases, the power consumption of the chopper rises a little and power efficiency decreases somewhat, as shown in Table 1.

This improved circuit can run at 96V to 260V ac (at 50 Hz). For a larger LED current, increasing the capacity of C_1 and decreasing the resistance of R_5

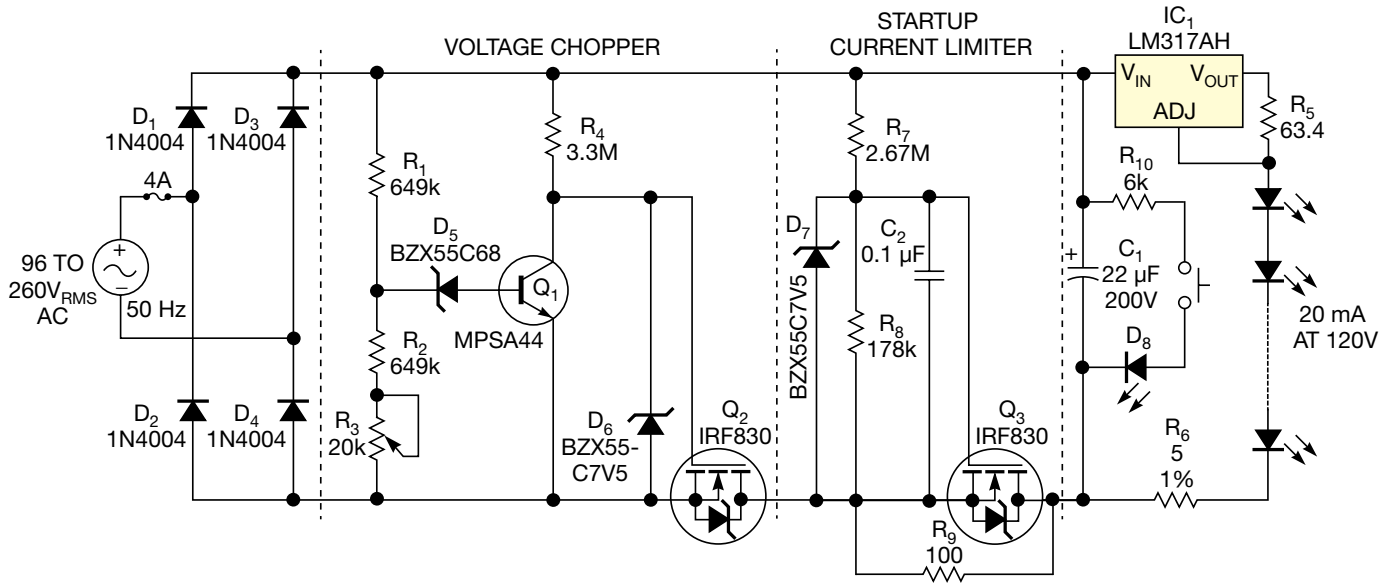


Figure 3 This circuit achieves an efficiency improvement by using tight control of the switching threshold to provide just barely enough LED voltage.

are suggested. For a different LED operation voltage, some parameters should be recomputed in the same way as in the foregoing analysis. The lower the LED operation voltage is, the lower the ac input voltage can be. This Design Idea can also apply to ac at 60 Hz.

1. Use high-voltage through-hole resistors or series surface-mount resistors to achieve at least 400V withstand. A fuse is suggested for safety against shorts.

2. Safety warning for novice experimenters: Lethal voltages are present in this circuit; use caution when testing and operating it. If scoping, use an isolation transformer to float the circuit's ac input from earth ground; do not float the oscilloscope chassis. The scope ground cannot be connected to the circuit without isolation.

3. Do not push the button with ac voltage applied. For safe maintenance, keep pressing the button to discharge C_1 through R_{10} until D_8 goes out. EDN

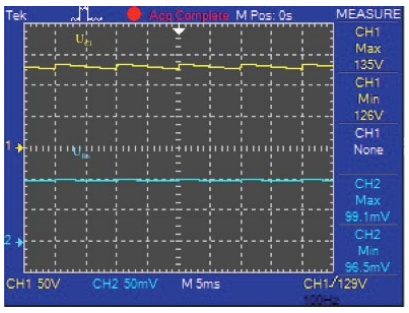


Figure 4 The yellow and blue traces, respectively, present the voltage across C_1 and R_6 in the circuit at $220V_{RMS}$ (at 50 Hz ac). The two traces remain at the same position when the ac input changes from $96V_{RMS}$ to $260V_{RMS}$.

REFERENCES

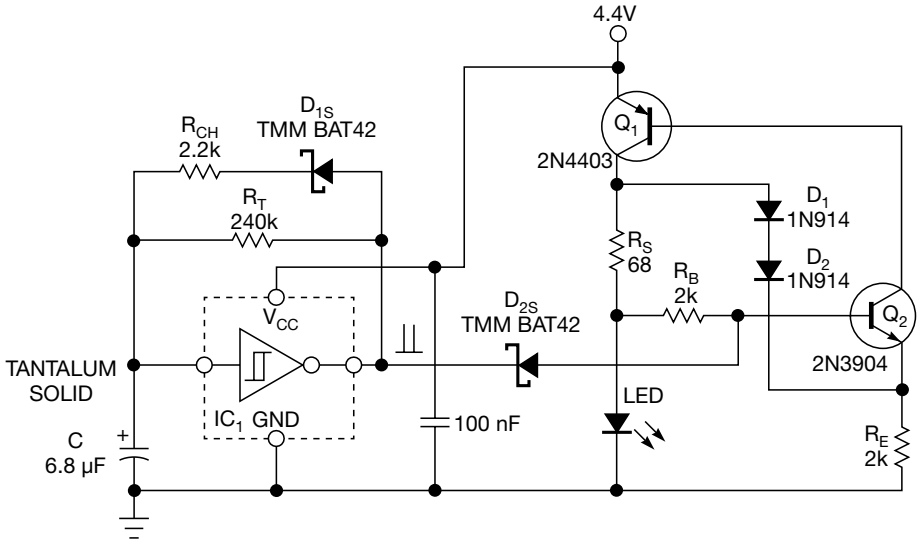
1 Sheard, Steve, "Driver circuit lights architectural and interior LEDs," EDN, Aug 11, 2011, pg 41, www.edn.com/4368306.

2 Babu, TA, "Offline supply drives LEDs," EDN, April 21 2011, pg 58, www.edn.com/4369648.

Low-duty-cycle LED flasher keeps power draw at 4 mW

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

Battery-operated equipment often will benefit from a power-on indicator. The indicator, however, can waste significant power. In situations where a low-duty-cycle blinking indicator provides an adequate indication of the power being turned on, the simple circuit described here should prove useful.



NOTE: LED IS A HIGH-RADIANCE TYPE.

Figure 1 Q_1 and Q_2 function as a current source and push a constant current through the LED regardless of its forward voltage drop (within the compliant voltage limitations). The Schmitt inverter forms a classic square-wave generator, modified with R_{CH} and D_{1S} to produce an asymmetrical output.

A tiny, single-gate Schmitt-trigger logic inverter, the SN74AHC1G14, together with two resistors, a Schottky diode, and a capacitor form the timing generator of the blinker, shown in Figure 1. The output waveform has a period of about 0.5 sec and a very low duty-cycle value, of around 1%. The interval of low-output duration, T_L, of the generator is expressed as

$$T_L = R_T C \times \ln\left(1 + \frac{2}{\frac{V_{CC}}{V_{HYST}} - 1}\right),$$

where V_{HYST} is the hysteresis voltage at the input of IC_1 and V_{CC} is the supply voltage of IC_1.

For V_{CC}=4.5V, the typical value for V_{HYST} is 0.75V. For the required value of T_L=0.5 sec, a value for R_T of 200k was selected. The value of the timing capacitor, C, can be calculated from the equation, with a small amount of algebraic rearranging, as 7.45 µF. The nearest standard value is 6.8 µF; a tantalum solid-electrolytic capacitor is used for this value.

To achieve the low duty cycle of the generator, the high-output duration, T_H, is shortened by speeding up the time to charge capacitor C. This is done through the additional resistor, R_{CH}, and the series-connected Schottky diode, D_{1S}. The forward voltage drop at D_{1S} is no more than 200 mV and can be neglected. The LED is on for approximately $(1/100)\times T_L \approx 5$ msec.

The LED driver comprises a PNP bipolar transistor, Q_1, and an NPN bipolar transistor, Q_2. Q_1 and Q_2 form a switchable current source. At a high logic level at the cathode of Schottky diode D_{2S}, a constant current flows through the LED with a value of roughly $I_O \approx 0.7V/R_S$, or about 10 mA in this circuit.

Series-connected silicon diodes D_1 and D_2 provide strong nonlinear negative feedback. If for any reason the voltage drop across the sensing resistor, R_S, rises, the D_1-to-D_2 connection will force almost the same increase in voltage at the emitter of Q_2. This increase reduces the collector current of Q_2 and, therefore, the base current of Q_1 and closes the loop; the net result is a reduction of the collector current of Q_1 to maintain a constant value.

Note that when the output of IC_1 goes low, the current through D_{2S} and resistor R_B is negligible. This is due to the fact that, with the output of IC_1 low, the base of Q_2 is held low, turning it and the current source off. With the current source off, the LED is off as well, and only microamps of leakage current flow through D_{2S} and R_B. If you use all surface-mount devices, you can build the circuit on a board no larger than 16×16 mm.

This work was supported by the Slovak Research and Development Agency under contract no. APVV-0062-11.EDN

Rotary encoder with absolute readout offers high resolution and low cost

Michael Korntheuer, Vrije Universiteit Brussel, Brussels, Belgium

Rotary encoders are typically used in positioning systems with servo feedback in which the cost of the encoder usually is of minor importance. Encoders, however, are also used in user interfaces to encode the positions of knobs—the volume knob on an audio system, for example. For those knobs, you have the choice between either a potentiometer boasting low cost, high resolution, and absolute readout but only limited travel—typically less than 340°—or a mechanical-optical rotary encoder, which has endless travel but a higher cost, low resolution, and only relative readout. The Design Idea presented here attempts to combine the advantages of the potentiometer with the endless operation of the mechanical-optical rotary encoder.

The encoder uses standard potentiometer construction techniques and is thus easily produced. It basically is a dual-wiper quadrature endless pot. It consists of a full ring of resistive material, which is powered from opposite sides and on which two electrically independent wipers move. The wipers are mechanically connected to each other at an angle of 90° (Figure 1).

An ADC on a microcontroller reads out the two signals; firmware uses both signals to determine in which quadrant the axis is located. Once the quadrant is known, the signal of both wipers can be used to calculate the position of the axis. When a wiper reaches the top or bottom power connections, its signal should be ignored because of nonlinear response (Figure 2). Both wipers cannot be in this nonlinear position at the same time because of the 90° angle between the wipers. Today, even the most basic microcontrollers offer a 10-bit ADC, so the combined signals give an 11-bit resolution, or better than 0.2°. The microcontroller can ignore the absolute readout if the application does not require it or when a software reset is useful.

This quadrature endless pot provides a user experience similar to the old tuning knob of a classical analog radio. It offers new possibilities in human-interface design and can give a quality feel in consumer products at low cost.EDN

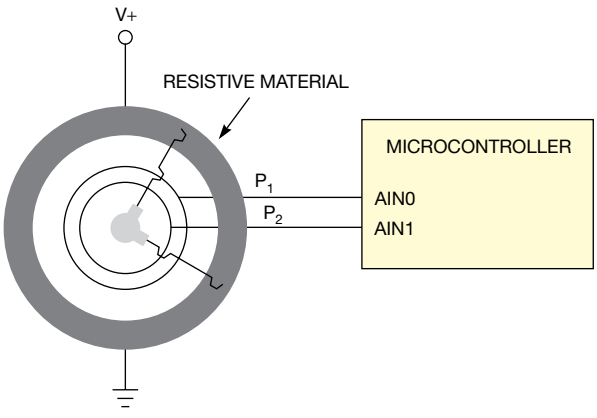


Figure 1 The encoder is a dual-wiper quadrature endless potentiometer that consists of a full ring of resistive material, which is powered from opposite sides and on which two electrically independent wipers move.

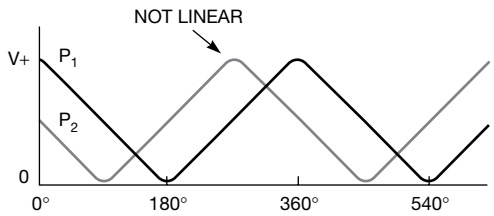
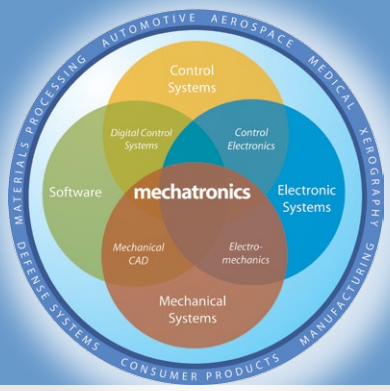


Figure 2 When a wiper reaches the top or bottom power connections, its signal should be ignored because of nonlinear response.



Forgotten practice loads costs of billions on to industry each year

Tribology—the science of friction, lubrication, and wear—must be rediscovered.

By Kevin C Craig, PhD

US engineering advancement has been catalyzed over the decades by external threats: the Space Race threat from the Soviet Union in the 1960s; the economic threat from Japan's low-cost, high-quality manufacturing in the 1970s; the demographic threat from post-World War II engineering retirements in the 1980s; the global threat as US competitiveness declined in the 1990s; and now the environmental threat driving the need for global energy conservation and sustainability. In addition, the impending retirement of the Baby Boom generation challenges the engineering profession, as these workers will take with them a vast amount of knowledge and skill that must be replaced.

One critical area, essential in manufacturing and transportation, is tribology, officially defined in 1966 as the science and technology of interacting surfaces in relative motion. An undergraduate engineering student receives less than one hour of instruction in tribology during a four-year program, so this matter demands urgent attention.

Tribologists, through the development of air-bearing technology between 1960 and 1980, enabled the extremely fast, reliable, precise, and accurate operation of a computer hard-drive read/write head (approximately 0.05×0.04×0.01 in.) riding over the disk surface on a cushion of air at a height of 15 nm and an average speed of 53 mph. The challenge for tribologists today is to understand the potential modes for wear and surface damage in an endless variety of mechanical systems.

Whether the goal is to reduce parasitic friction or enhance friction in a design, the designer must employ a proper tribological approach—the right combination of geometry, materials, and lubrication—to ensure safety, performance, and energy-efficient operation. Estimates are that the correct application of tribology throughout US industry could save $500 billion annually.

Friction, inevitably accompanied by wear, accounts for most of the energy consumed in our society. The object of lubrication is to reduce friction, wear, and heating of machine parts, which move relative to each other. A lubricant is any substance that, when inserted between moving surfaces, accomplishes those purposes.

Several types of lubrication exist: Hydrodynamic refers to full-fluid-film lubrication, hydrostatic refers to lubricant introduced under pressure to create a full film, elastohydrodynamic refers to lubricant films between elastically deformable surfaces, boundary refers to a fluid film several molecular dimensions thick, and solid refers to solid lubricants used at high temperatures. Unlubricated surfaces have a friction coefficient of about 1.0 with heavy wear; for boundary and thin-film lubrication, the value is about 0.01 with slight wear; and for thick-film lubrication, the value is about 0.001 with no wear.

The most common fluid-film bearing is the journal bearing, in which a sleeve of bearing material is wrapped partially or completely around a rotating shaft to support a radial load. Figure 1 shows a plot of the coefficient of friction versus Hersey number (μN/P, where μ is the absolute viscosity in centipoise, N is the shaft speed in rpm, and P is the average pressure in psi) for a journal bearing under test conditions, and is a good measure of the state of health of the bearing.

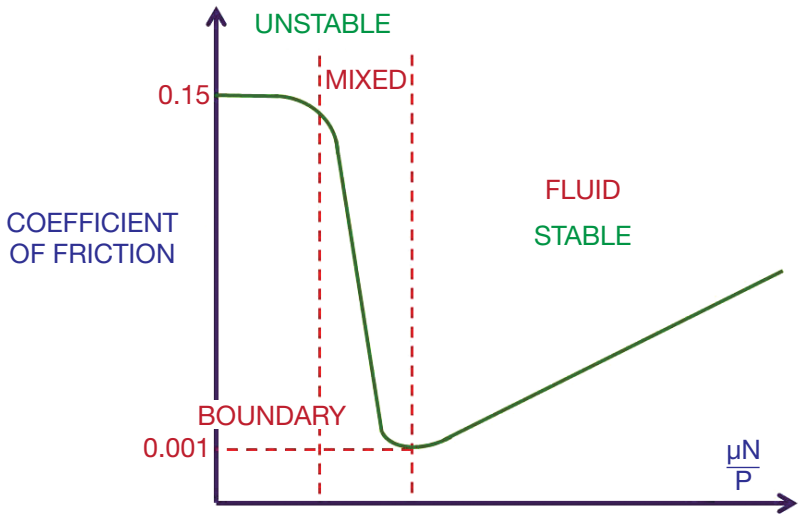


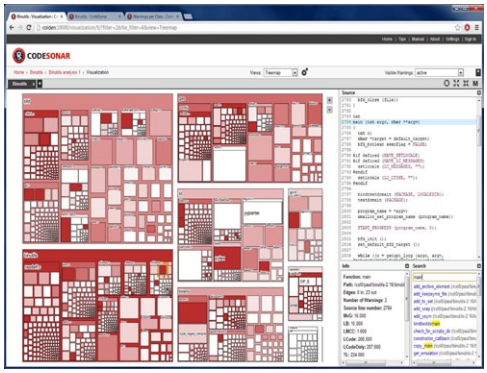
Figure 1 This plot of the coefficient of friction versus Hersey number for a journal bearing under test is a good measure of the health of the bearing.

There are other areas of science and technology that, like tribology, are threatened. Once these skills and knowledge are lost, getting them back will be nearly impossible. EDN

productroundup

Code analysis visualisation

GrammaTech's CodeSonar software-analysis tool has acquired extended software architecture visualisation features, including a new treemap view designed to allow users to see the hierarchical structure of the code in a very information-dense form. The view colour-codes density of defects in modules to highlight the most problematic parts of the code. The call graph is organised by module structure. Users can drill down to see a greater level of detail, choose different layouts such as treemap, circuit, cluster, flow, radial and other layouts, and attach persistent notes to the diagram. Transitions such as zooming or layout changes are fluid and real-time. Users can start at individual functions to gain insight from a bottom-up perspective, annotate nodes and edges with additional information and, overlay the visualisation with information on defects and source-code metrics.



GrammaTech, www.grammatech.com

Dual-core A9 image processor

Under the branding "Visconti 3" Toshiba has added a line of image-recognition processors for automotive use, targeting functions such as recognition of traffic lanes, vehicles, pedestrians, and traffic signs using integrated image processing accelerators that detect pedestrians with high level detection ratio, in real time. The first device in the series, TMPV7528XBG, incorporates an ARM 32-bit Cortex-A9 MPCore in dual-core configuration, for applications-interfacing with the image recognition processor. To optimise image recognition algorithms that analyse large volumes of image data from the video source, frame-by-frame, in real time, but with limited power consumption and memory resources, Toshiba has configured the Cortex-A9 cores with a single/double-precision FPU in each core. Also on-chip is a Toshiba 32-bit RISC CPU; a media embedded processor (MeP); four instances of Toshiba's multi-core media processor Media Processing Engine (MPE); and hardware accelerators for specific functions.

Toshiba Electronics Europe, www.toshiba-components.com

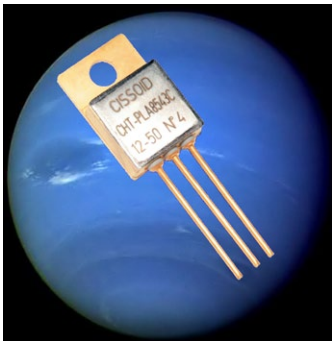
AMD G-Series embedded PC

For industrial and embedded computing applications, MEN's BC50I uses an AMD Embedded G-Series Dual Core G-T48N APU, features two Gigabit Ethernet ports, two USB 2.0 ports and two DisplayPorts. It supports a wide range of communications standards and includes "legacy" serial communications, as well as an optional CAN bus connection. It is conduction cooled and rated for operation over -40 to +70°C. Processor core frequency is 1.4 GHz, and other AMD Embedded G-Series can be selected for alternative processing power points. The DisplayPorts with a maximum resolution of 2560x1600 pixels each deliver HD quality. The BC50I has a 16 to 36 V wide-range power supply and costs €995 (single unit).

MEN, www.men.de/09BC50I.html

1200V, 225°C SiC MOSFET

CHT-Neptune is a high-voltage silicon carbide power switch in a TO-257 package, suitable for power converters and motor drives and guaranteed for reliable operation up to +225°C. The package has junction-to-case thermal resistance of 1.1°C/W; the device has a breakdown voltage in excess of 1200V and will switch currents up to 10A at the maximum temperature (Tj=225°C). The device features a body diode that can be used as free-wheeling diode. The switch can be controlled with a typical gate voltage (VGS) of -2V / +20V. The transistor's RDS-ON is 90mΩ at 25°C and 150mΩ at 225°C with VGS=20V. Support and characterisation data can also be provided to drive the transistor at lower VGS voltages (e.g. 5V or 10V). This new device features low - and temperature-independent - switching energy of less than 400µJ at 600V/10A. Pricing is €287.38 (51 – 200).



Cissoid, www.cissoid.com

Ultra-low noise regulators

The PS2292X series are robust linear regulator products built in a bipolar process for low noise performance and very low dropout (LDO) current. The devices are part of a high current, single supply, LDO family that operates from an input voltage as low as 1.7V and as high as 12V, for use in low voltage, post regulation applications. They have fast transient response while maintaining high Power Supply Rejection Ratio (PSRR). Other fea-

tures include adjustable and fixed voltage output options, ON/OFF control, power-good with 500 µsec delay, bypass pin for ultra-low noise, over temperature and over current protection. They are rated over -40°C to 125°C junction temperature, and are stable with small ESR ceramic capacitors. The three parts in this release are PS22921, PS22922 and PS22924, respectively delivering 0.5, 1.0 and 2.0A from packaging styles of SOT23-5, SOT223 and SOIC-8 EDP. Prices are in the region of 5 to 15 US cents depending on specification and volume.
Plessey, www.plesseysemiconductors.com

Low phase noise TCXO

IQD's IQXT-60 series temperature compensated crystal oscillator (TCXO) has typical phase noise figures of -63 dBc/Hz at 10 Hz and -161 dBc/Hz at 100 kHz, coupled with a low current consumption of around 5.0 mA. In a miniature 3.2 x 2.5 mm ceramic package measuring only 1.0 mm high, the new model is available at any frequency from 4.0 MHz to 54.0 MHz; this is wide for a TCXO and removes the need for external dividers or multipliers in many applications. The frequency stability of ±2.5 ppm over the operating temperature range of –30 to +75C and frequency tolerance of ±0.5 ppm matches existing industry standards. The IQXT-60 series has an HCMOS output capable of driving 15 pF whilst operating from a standard 3.3, 2.8 or 2.5V power supply.

IQD, www.iqdfrequencyproducts.com

High-speed, low-density CMOS SDRAM

Alliance Memory has introduced a high-speed CMOS synchronous DRAM (SDRAM) with a low density of 16 Mb in a 50-pin, 400-mil plastic TSOP II package. The AS4C1M16S offers access time from clock of 5.4 nsec at a 7-nsec clock cycle, and a clock rate of 143 MHz. The part is intended for applications requiring high memory bandwidth, such as high-performance PC applications. Internally configured as dual banks of 512K word x 16 bits with a synchronous interface, the SDRAM operates from a single +3.3-V (±0.3V) power supply. The AS4C1M16S provides programmable read or write burst lengths of 1, 2, 4, 8, or full page, with a burst termination option. An auto precharge function provides a self-timed row precharge initiated at the end of the burst sequence. Refresh functions include auto- or self-refresh, while a programmable mode register allows the system to choose the most suitable modes to maximize performance. Alliance Memory's "legacy" ICs provide reliable drop-in, pin-for-pin-compatible replacements for a number of similar solutions.
Alliance Memory, www.alliancememory.com.

IGBT/SiC FET gate drivers

TI has announced 35-V, single-channel, output stage power management gate drivers for insulated-gate bipolar transistors (IGBTs) and silicon carbide (SiC) FETs. UCC27531 and UCC27532 output stage gate drivers with split output claim the most efficient output drive capability, shortest propagation delay and increased system protection for isolated power designs, such as solar inverters, uninterruptible power supplies and electric vehicle charging. Next-generation IGBT- and SiC FET-based designs require both power and signal isolation from the noisy switching environment of the power stage. UCC27531 features output drive capability of peak current of 2.5A source and 5A sink, allowing fast charging of IGBTs. It has 17 nsec typical propagation time, provides UVLO settings and rail-to-rail output voltage, and handles noisy environments – negative input voltage handling allows the driver to support many industrial designs. Split-output configuration improves Miller turn-on immunity and prevents damage of IGBT/MOSFET. The UCC27531 and UCC27532 come in a 6-pin, SOT-23 package priced at $0.75 (1,000). The UCC27531EVM-184 IGBT driver daughter card evaluation module is priced at US$49: a PSpice model and application note "35-V single-channel gate drivers for IGBTs" is available.
Texas Instruments, www.ti.com/ucc27531-pr-eu

Optical T-o-F proximity sensor

Intended to solve a particular problem in smartphone design, ST has introduced a combined proximity and ambient light sensor that delivers fast, accurate and reliable sensing under the most difficult conditions. It uses time-of-flight measurement, of pulsed infra-red light, to accurately measure distance to a nearby object with high reliability: built-in ambient light sensing ensures that it works under all lighting conditions. Combining three optical elements in a single package, the VL6180 is the first member of ST's FlightSense family: optical-sensing technology can reduce the incidence of dropped calls and enables new user interactions with smartphones, ST says. It enables accurate and reliable calculation of the distance between the smartphone and the user. Instead of estimating distance by measuring the amount of light reflected back from the object, which is significantly influenced by colour and surface, the sensor precisely measures the time the light takes to travel to the nearest object and reflect back to the sensor – the first time this has been done in a form factor small enough to integrate into a product such as a smartphone.

STMicroelectronics, www.st.com

Ultra-low power 32-bit RX MCUs

Renesas is expanding the RX family of microcontrollers to include the lowest power, lowest cost RX 32-bit MCU for the embedded market, integrating as little as 8 KB of flash memory. The RX100 Series MCUs, which are based on a proven 130nm, low-power process technology, can run at 32MHz, delivering 1.56 DMIPS/MHz throughput, consuming only 110 µA/MHz power in full active mode and targeting only 350 nA in the standby mode. This achieves an even lower cost and power consumption than the RX200 series already in the market. The RX100 series is intended for low power applications such as wearable/battery powered applications including medical and sensor products. The very figure of 350 nA current consumption and 70 µA/DMIPS is the kind of power consumption typically only found in the 8-bit market, Renesas claims. Samples of the RX100 offering flash memory integration from 8 KB to 128 KB, are now available and mass production is scheduled for 4Q of 2013.
Renesas Electronics Europe, www.renesas.eu. ne

FRANK W BELL • KYBERNETIX LLC

Nonlinear transmission lines keep developer on the fence

In 1982, I was developing a phone and telemetry system to operate on New Zealand farmers' electrified fences. The controller that generated the jolt was usually a mains-powered pulse generator, and better units produced mostly unipolar pulses of up to 5 kV for a duration of about 20 msec, repeated about once a second—not lethal, but enough to kill any notion of touching the fence again. The high voltages were even effective on unshorn, woolly sheep.

Such a fence behaves as an earth-return transmission line with an impedance of around 600Ω, depending on construction. The system polarity is decided based on resistance to lightning, which usually consists of negative current into the fence from a direct strike, though positive current may come from a strike nearby. The system I was developing used biased blocking diodes to prevent the pulse from frying the electronics (not to mention avoiding the loud click in the ear). Detection of a dc bias on the fence turned on a DTMF decoder to select the receiver.

Field trials were essential. On one farm, the DTMF decoder provided an output burst a couple of times and then died. Testing with a blocking diode and oscilloscope showed a positive pulse of 12 µsec after the negative controller pulse. Assuming a velocity factor of 0.7, that gave a range of 1.25 km, or about three-quarters of a mile. When I checked the fence leakage to ground, however, it was more than 3 kΩ for the whole farm. The controller included a circuit to eliminate positive pulses. How could a low impedance have inverted the pulse polarity?

I drove out in a truck to the 1.25-km distance on the odometer. I didn't see any stray wires going into the ground, a common problem. When I got out of the truck, though, I noticed an audible click with a 1-sec interval.

I took a look at the fence. The farmer had used steel posts and had cut lengths of plastic hose, with a lengthwise slit, for insulators. A thin wire tied the hose to the post. Though there was insulation, the air gap was breaking down with the pulse from the controller and producing a positive polarity reflection. I explained the problem to the farmer, who later installed proper insulators and told me the fence worked "much better now."

After diagnosing the cause of the failure of my prototype electric fence telephone/DTMF controller, I installed additional clamping so that positive pulses would not reach the DTMF decoder. Normally, farmers did their testing without any instruments—though perhaps with rubber gumboots—by touching the fence and a blade of grass, but testing in this environment required battery-powered oscilloscopes, as the voltage on the grounding points could easily exceed the rated insulation of the mains-powered equipment. The educational material for the controller installation made it clear that the controller ground had to be well separated from the ground of the ac mains because of such voltages.

On another farm, connections between phones along the fence were intermittently dropping out between controller pulses. I checked out the fence, which was so rusty that I had to work the alligator clips—with insulated pliers, of course—to get a connection to the metal underneath. The connections between wires were simply loops holding loops. These also were rusty connections, and the arc of the pulse temporarily welded the wires together. Poor connections also cause AM radio interference when they get rusty. The farmer replaced the rusty fence, which was becoming unreliable anyway.

In order to examine the high-voltage pulses, we modified a Heathkit TV high-voltage probe using a capacitor made from car-ignition cable with a metal conductor, a braid on the outside, and a divider and a compensation circuit to correct the square waves from a calibration source (tube scope) of higher-than-normal voltage. The Tektronix EHT probe would have been better, but it wasn't affordable.

The patent for the telemetry system eventually expired without resulting in a successful product. EDN

Frank W Bell is president of Kybernetix (Clifton, NJ).